

FIG. IA

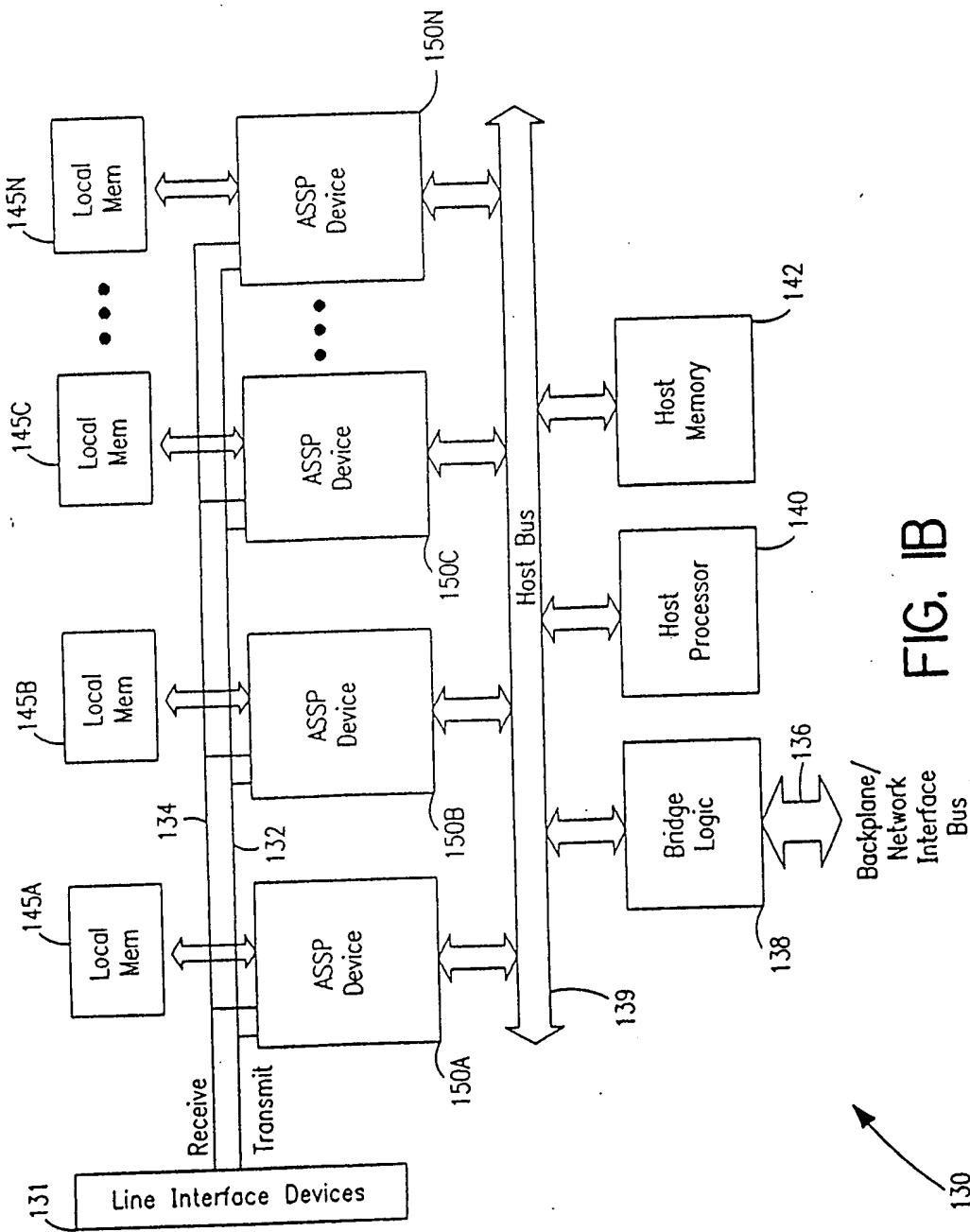


FIG. 1B

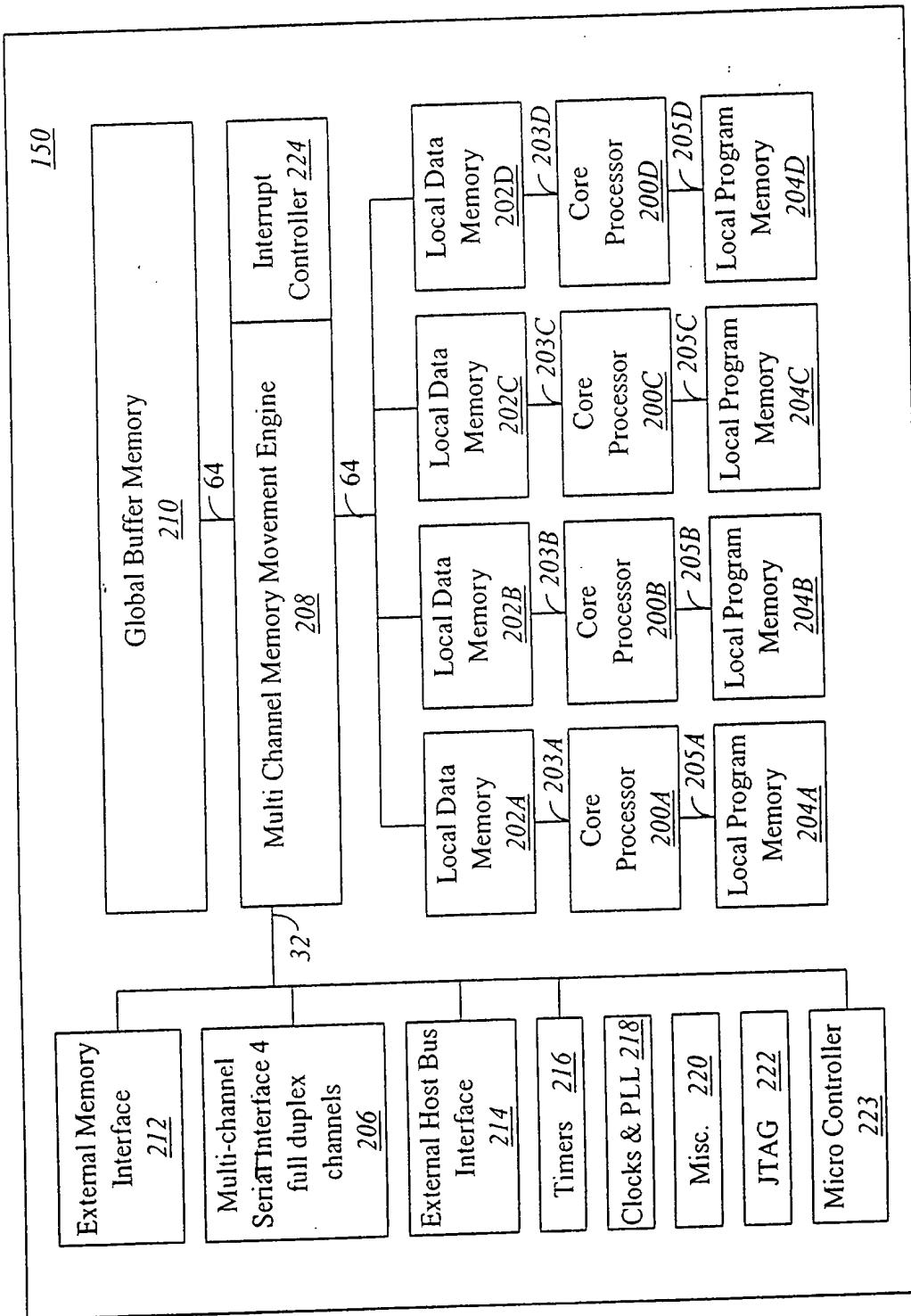


FIG. 2

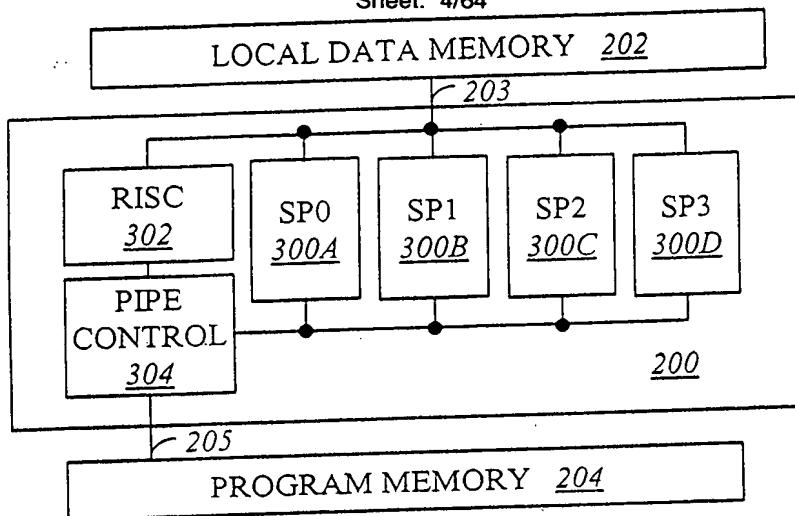


FIG. 3

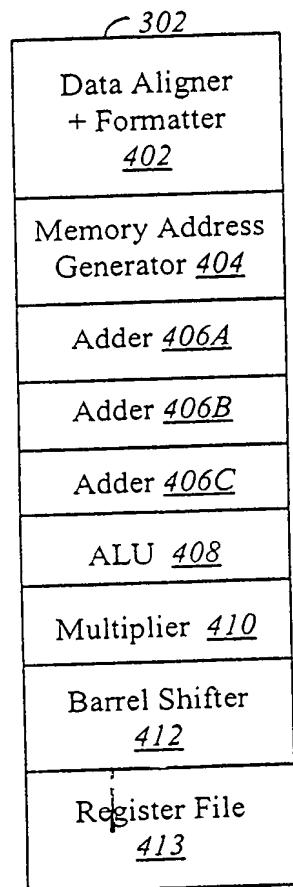


FIG. 4

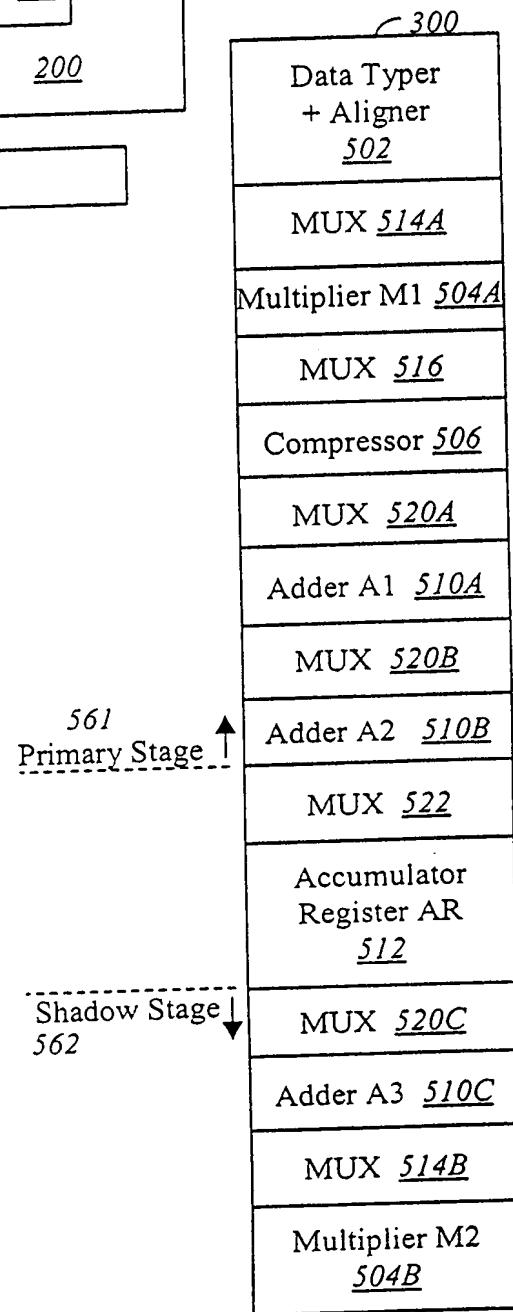


FIG. 5A

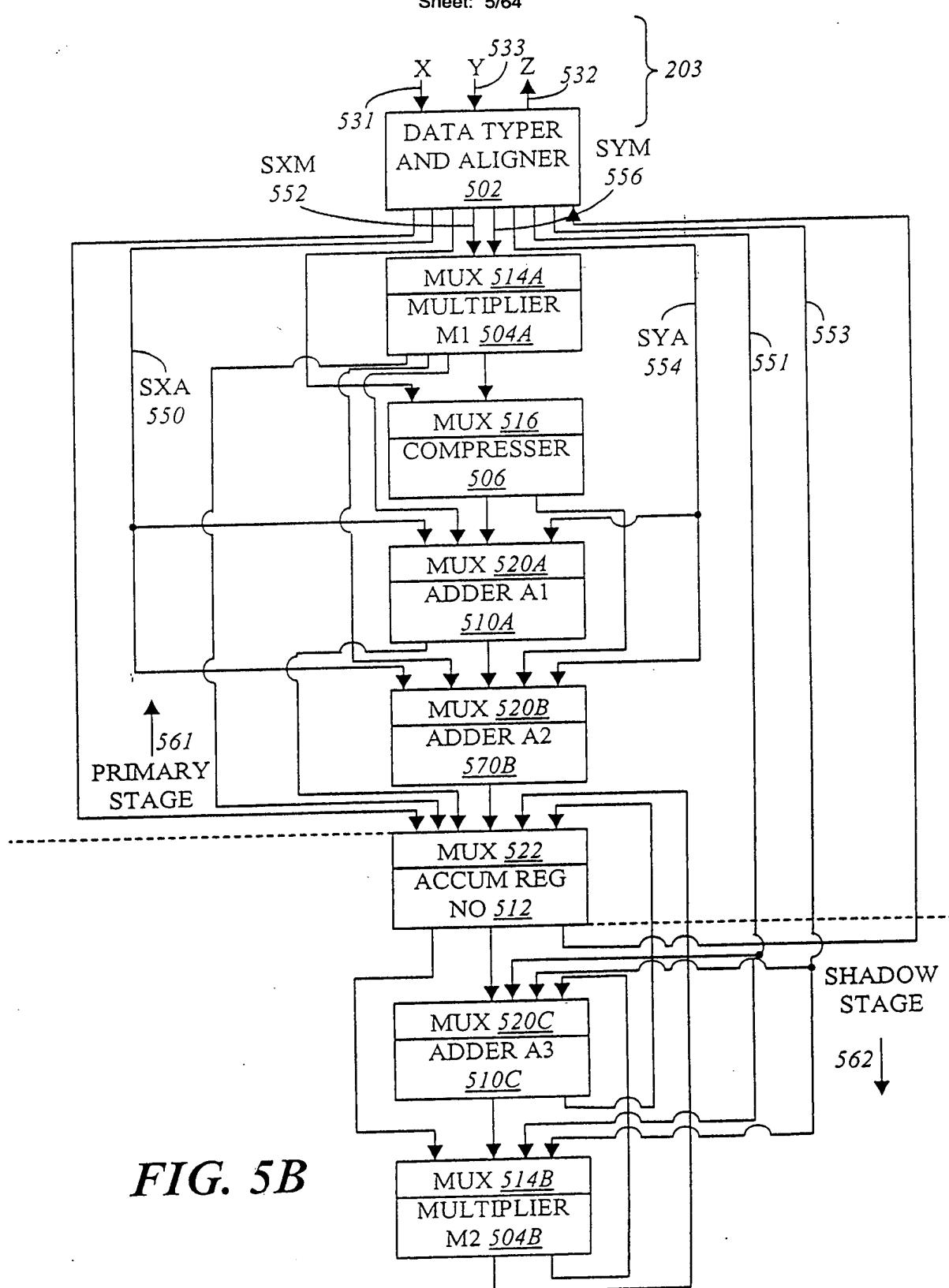


FIG. 5B

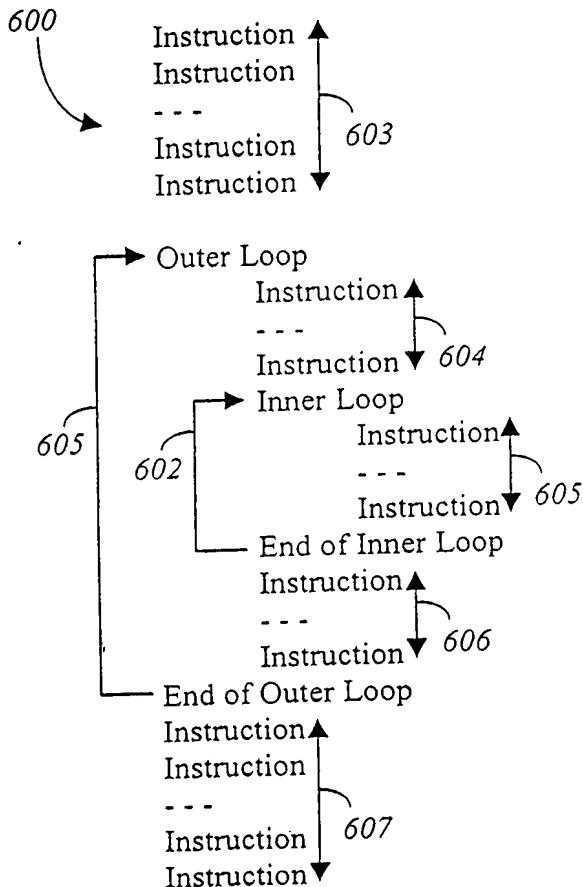


FIG. 6A

610	
611	612
MAIN OP	SUB OP
MULT	NOP
ADD	MIN/MAX
MIN/MAX	ADD
NOP	MULT

FIG. 6G

<u>20-bit ISA</u>	<table border="1"> <tr> <td>39</td><td>19</td></tr> <tr> <td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td></tr> <tr> <td>1</td><td>0</td></tr> <tr> <td>1</td><td>1</td></tr> </table>	39	19	0	0	0	1	1	0	1	1	20-bit parallel	Control II Control
39	19												
0	0												
0	1												
1	0												
1	1												
		20-bit serial	Control # Control										
		40-bit extended	DSP, extensions/Shadow										
		20-bit serial	DSP # DSP										

FIG. 6B

6-bit operand specifier:

A 6-bit specifier is used in DSP extended instructions to access memory and register operands.

5	4	3	2	1	0
---	---	---	---	---	---

M/R

0	0	ac-page
0	1	gpr:0-r15
1	ptr(r0)to(r15)	off

ereg

GPR

Mem[ptr{0-15}]II PTR[0-15]+=offset1/offset2 Always postupdate

This allows access to data memory, ereg and GPR

- Bit 5=1: Use rX(X:0-7) register to obtain effective memory address and post-modify the

ptr field by one of two possible offsets specified in rX registers.

dmem[ptr], ptr=ptr+offset1, if off=0
 ptr=ptr+offset2, if off=1
- Bit 5=0: Access ac-page or GPR

If Bit-4 is set to 0, then bits 3:0 control access to the general-purpose register file (r0-15) or to execution unit registers.

ereg-Shadow				
GPR	GPR Intr page	ac-page	ac intr page	DSP
R0	R0	A0	A0 I	A0
R1	R1	A1	A1 I	A1
R2	R2	T	T	T
R3	R3	TR	TR	TR
R4	R4			
R5	R5			
R6	R6			
R7	R7			
R8	R8			
R9	R9			
R10	R10			
R11	R11			
R12	R12 i			
R13	R13 i			
R14	R14 i			
R15	R15 i			

FIG. 6C

4-bit operand specifier:

Memory operands: (rX) specifies an access out of the data memory to the extension unit for the function that needs to be performed. The address for the access is specified in the rX register in the general register file that hold the 14-bit pointer (16K of addressing) to memory, 5-bit signed offset or a 3-bit unsigned offset that can post-modify the address. In addition, each pointer is typed for efficient SIMD processing and includes a permute control for rearranging data elements of a vector on the fly. The “podi” core can deal with 4-element 16-bit real vectors or complex data directly. This ability to manipulate memory data directly reduces the instruction width greatly and allows efficient signal processing.

(rX): Memory Address Registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
type	cb	x	permute	off1:(0-7)	off0:(-16 to 15)																									ptr: pointer	

Fig. 6D

For shadow DSP instructions, the 3-bit specifier for operands is defined as follows:

<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>2</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	2	1	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	EREG1	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>2</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	2	1	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	1	1	0	1	1	1	EREG2
2	1	0																																																							
0	0	0																																																							
0	0	1																																																							
0	1	0																																																							
0	1	1																																																							
1	0	0																																																							
1	0	1																																																							
1	1	0																																																							
1	1	1																																																							
2	1	0																																																							
0	0	0																																																							
0	0	1																																																							
0	1	0																																																							
0	1	1																																																							
1	0	0																																																							
1	0	1																																																							
1	1	0																																																							
1	1	1																																																							
A0		A0																																																							
A1		A1																																																							
T		T																																																							
TR		TR																																																							
SX1		SY1																																																							
SX1s		SY1s																																																							
SX2		SY2																																																							
SX2s		SY2s																																																							

Only the shadow DSP instructions can see the above modified page of execution unit registers.

FIG. 6E

REPLACEMENT SHEET

**Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT**

1st Named Inventor: Ruban Kanapathippillai

Application No.: 10/649,067 Docket No.: 42P14037D2

Sheet: 9/64

5-bit operand specifier:

The 5-bit specifier includes the 4-bit specifier for general data operands and the special purpose registers. It is used in RISC instructions.

4	3	2	1	0
0	spr:s0-s15			
1	gpr:r0-r15			

SPR	Intr page
SPR	SPR intr page
0 fu-ctl	fu-ctl_l
1 a-type	a-type_l
2 ps-ctl	ps-ctl
3 t-type	t-type
4 pl-ctl	pl-ctl
5 cb-ctl	cb-ctl_l
6 shuffle	shuffle
7 lo-ptr	lo-ptr
8 status	status_l
9 loop-ctl	loop-ctl
10 pcr	pcr
11 reserved	reserved
12 reserved	reserved
13 reserved	reserved
14 reserved	reserved

NOTE: All SPR registers are reset to all zeros at power on reset except for the PCR register.

FIG. 6F

DSP instructions

39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20

	1	0	0	PS	S'	SX	SY	V/SSA	DA	Sub-op	
Multiply						da=sx*sy				0 0 0	Nop
						da=(sx*sy)+sa				0 0 1	Add
						da=(sx*sa)+sy				0 1 0	Add
						da=(sx*sy)+sa				0 1 1	Sub
						da=(sx*sa)+sy				1 0 0	Sub
						da=min(sx*sy,sa)				1 0 1	Min
						da=min(sx*sa,sy)				1 1 0	Min
						da=max(sx*sy,sa)				1 1 1	Max
Add	1	0	1	PS	+/	SX	SY	V/SSA	DA	Sub-op	
						da=sx+sy				0 0 0	Nop
						da=sx+sy+sa				0 0 1	Add
						da=sx+sy; sa=sx+sy;				0 1 0	AddSub
						da=(sx+sy)*sa				0 1 1	Mul
						da=-(sx+sy)*sa				1 0 0	MulN
						da=min(sx+sy,sa)				1 0 1	Min
						da=max(sx+sy,sa)				1 1 0	Max
						da=ssum(sa) (sx,sy unused)				1 1 1	CombAdd
Extremum	1	1	0	PS	x/n	SX	SY	V/SSA	DA	Sub-op	
						da=ext(sx,sy)				0 0 0	Nop
						da=ext(sx,sy,sa)				0 0 1	Ext
						da=ext(sx,sa)*sy				0 1 0	Mul
						da=-ext(sx,sa)*sy				0 1 1	MulN
						da=ext(sx,sa)+sy				1 0 0	Add
						da=ext(sx,sa)-sy				1 0 1	Sub
						ext(sa,da) ?1=sx,tr=sy,lcs=lc				1 1 0	amax
type-match	1	1	0	PS	0	SX	SY	x	x	x	1 1 1
Permute	1	1	0	PS	0	x x x x x	x x x x x	x	x	x	1 1 1
Reserved	1	1	0	PS	1	Type	SY	0	ereg	1 1 1	Permute
	1	1	1	PS	x	SX	SY	SA	DA	V/S	Sub-op

FIG. 6H

Control and specifier Extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

Mul	0	Pred	PL	Sxt	Syt	Rnd	Lt	S'	S'	S'	0	SA	DA	abs	0	0	0	0
-----	---	------	----	-----	-----	-----	----	----	----	----	---	----	----	-----	---	---	---	---

Add	0	Pred	PL	Sxt	Syt	Lt	Sub-ext	0	SA	DA	abs	0	0	0	0	0	0	0
-----	---	------	----	-----	-----	----	---------	---	----	----	-----	---	---	---	---	---	---	---

+/	+	+	-	-	x
x	V	S	Rnd	Fp	
tr/ctl	Gx	Fp			

Nop (uadd)
 Mul/MulN
 Min/Max

Ext	0	Pred	PL	Sxt	Syt	tr-ctl	Gx	Sub-ext	0	SA	DA	abs	0	0	0	0	0	0
-----	---	------	----	-----	-----	--------	----	---------	---	----	----	-----	---	---	---	---	---	---

Lt	Fp
Rnd	V/S

Add/sub
 Mul

0	Pred	PL	Sxt	Syt		Pctl1	0	ereg	Pctl	0	0	0	0	0	0	0	0	0
---	------	----	-----	-----	--	-------	---	------	------	---	---	---	---	---	---	---	---	---

Type/offset/permute extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Pred	PL	x	Type:SX		Type:SY	0	SA	DA	x	0	1							
0	Pred	PL	Psx	Permute:SX		Permute:SY	0	SA	DA	Psy	1	0							
0	Pred	I/R	I/R	prX	Offset:SX	Offset:SY	0	SA	DA	prY	1	1							

Type override
 permute override
 Offset override

Shadow DSP

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Op	PL	Op	SA	ereg1	DA	ereg2	1	SA	DA	Sub-op								
---	----	----	----	----	-------	----	-------	---	----	----	--------	--	--	--	--	--	--	--	--

nop

1	1	0	PL	0	x	x	x	Rnd	x	x	x	x	0	SA	DA	1	1	1
---	---	---	----	---	---	---	---	-----	---	---	---	---	---	----	----	---	---	---

FIG. 61

Control instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add,sub	L	Pred	0	0	0		RX				RY			!	RZ	+/-	0			
max,min	L	Pred	0	0	0		RX				RY			!	RZ	X/N	1			
Shift	L	Pred	0	0	1		RX				UI4			!	RZ	UI2	R/L			
Logic	L	Pred	0	1	0		RX				RY			RZ	&	&1				
Mux	L	Pred	0	1	1		RX				RY			RZ		Pd	0			
mov	L	Pred	0	1	1		RX				DZ			Rxt	Dzl	0	0	0	1	
addi	L	Pred	0	1	1		SI4				DZ			x	x	1	0	0	1	
mov2erg	L	Pred	0	1	1		RX				unit	ereq		qd	type	1	0	0	1	
I.dm	L	Pred	0	1	1		RX				DZ1			DZ2			1	1		
Set4bits	L	Pred	1	0	0		UI4:POS				RY			Rzt		UI4		0		
Set2bits	L	Pred	1	0	0		UI4:POS				RY			Rzt	UI2	0	0	0	1	
Setbit	L	Pred	1	0	0		UI4:POS				RY			Rzt	UI1	UI1	1	0	1	
Movi	L	Pred	1	0	0						SI8			RZ			1	1		
Jmp	L	Pred	1	0	1						SI9			0	PRED	0	0			
Call	L	Pred	1	0	1						SI9			1	PRED	0	0			
Loop	L	Pred	1	0	1		UI5:Lcount				UI5:Lsize			UI2:Lst	0	1				
Jmpi	L	Pred	1	0	1		RX				x	x	x	x	x	0	PRED	1	0	
Calli	L	Pred	1	0	1		RX				x	x	x	x	x	1	PRED	1	0	
Loopi	L	Pred	1	0	1		RX				x		UI5:Lsize		UI2:Lst	1	1			
Test	L	Pred	1	1	0		RX				RY			PZ	=,<,>	0				
Testbit	L	Pred	1	1	0		RX				UI5			PZ	B	0	1			
Andp, orp	L	Pred	1	1	0		Pa				Pb			Pc		PZ	&	1	1	
Load	L	Pred	1	1	1		MX				RZ			Ext	0	0	0			
Store	L	Pred	1	1	1		MZ				RZ			Ext	1	0	0			
eLoad	L	Pred	1	1	1		MX				RY			1	1	1	0	0	0	
eStore	L	Pred	1	1	1		MZ				RY			1	1	1	1	0	0	
Extended	L	Pred	1	1	1									Bits 27:16			1	0		
Logic2	L	Pred	1	1	1		RX				RY/RZ			Rxt	Ryt	&,1,&1,1	0	1		
mov-erg	L	Pred	1	1	1		unit	ereq			RZ			qd	Sft	0	1	1	1	
Crb	L	Pred	1	1	1		RX				RZ			s/m	0	0	1	1	1	
Panty	L	Pred	1	1	1		RX				PZ			I/O/E	0	1	0	1	1	
Stm	L	Pred	1	1	1		MZ				RY			1	1	0	1	1	1	
Abs	L	Pred	1	1	1		RX				RZ			0	0	1	1	1	1	
Neg	L	Pred	1	1	1		RX				RZ			0	1	1	1	1	1	
Div-step	L	Pred	1	1	1		RX				RZ			1	0	1	1	1	1	
Test&Set	L	Pred	1	1	1		RX				PZ			0	1	1	1	1	1	
Reserved	L	Pred	1	1	1						0	0	1	1	1	1	1	1	1	
Return	L	Pred	1	1	1		Pred	I-ctl	0	1	0	1	1	1	1	1	1	1	1	
Zero-ac	L	Pred	1	1	1		ac #		1	1	0	1	1	1	1	1	1	1	1	
eSync	L	Pred	1	1	1		RZ		0	1	1	1	1	1	1	1	1	1	1	
Swi	L	Pred	1	1	1		UI3	0	1	1	1	1	1	1	1	1	1	1	1	
Nop	L	Pred	1	1	1		UI3	1	1	1	1	1	1	1	1	1	1	1	1	

<Bit1,Bits9-6>
 ==UI5 (Shift Amount)

<Bit3,Bits13-10>==UI5 POS

FIG. 6J

Extended Control

jmp, call	dloop	dloopi	mult	add/sub	Reserved	logicp	Testi	Movi	loadi	storei	loadt	storet	Addi/subi	mini/maxi	andi/on
-----------	-------	--------	------	---------	----------	--------	-------	------	-------	--------	-------	--------	-----------	-----------	---------

FIG. 6K

REPLACEMENT SHEET
Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT
1st Named Inventor: Ruban Kanapathippillai
Application No.: 10/649,067 **Docket No.: 42P14037D2**
Sheet: 14/64

MAC:		ARITH:												EXT:												LOGIC:																		
Group	Pred	opcode	SX				SY				DZ				SX				SY				DZ				SX				SY				DZ									
1-40-bit																																												
2-20 set																																												
2-20 par																																												
res.																																												
ARITH:	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Group	Pred	opcode																																										
EXT:	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Group	Pred	opcode																																										
LOGIC:	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Group	Pred	opcode																																										

FIG. 6L-1

Shift:		39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
Group	Pred	opcode	---	SX	DZ	Amount	PL	PS	Lt	Rot	Fill	A/L	1	Shift			
Group	Pred	opcode	---	SX	DZ	Amount								I/E	0	1	Insert/extract
Group	Pred	Imm2	opcode	DZ	Imm14	Length								Setbits	0	0	Position
Immediate:		39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
Group	op	DZ			Imm32												
Group	opcode		SX	DZ	Subop	MOV	ADD	SUB	MIN	MAX	AND	OR					Imm16
Test:		39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
Group	Pred	opcode	SX	St	Dp2	Subop											Imm20
Branch:		39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
Group	Pred	opcode															
Misc:																	

FIG. 6L-2

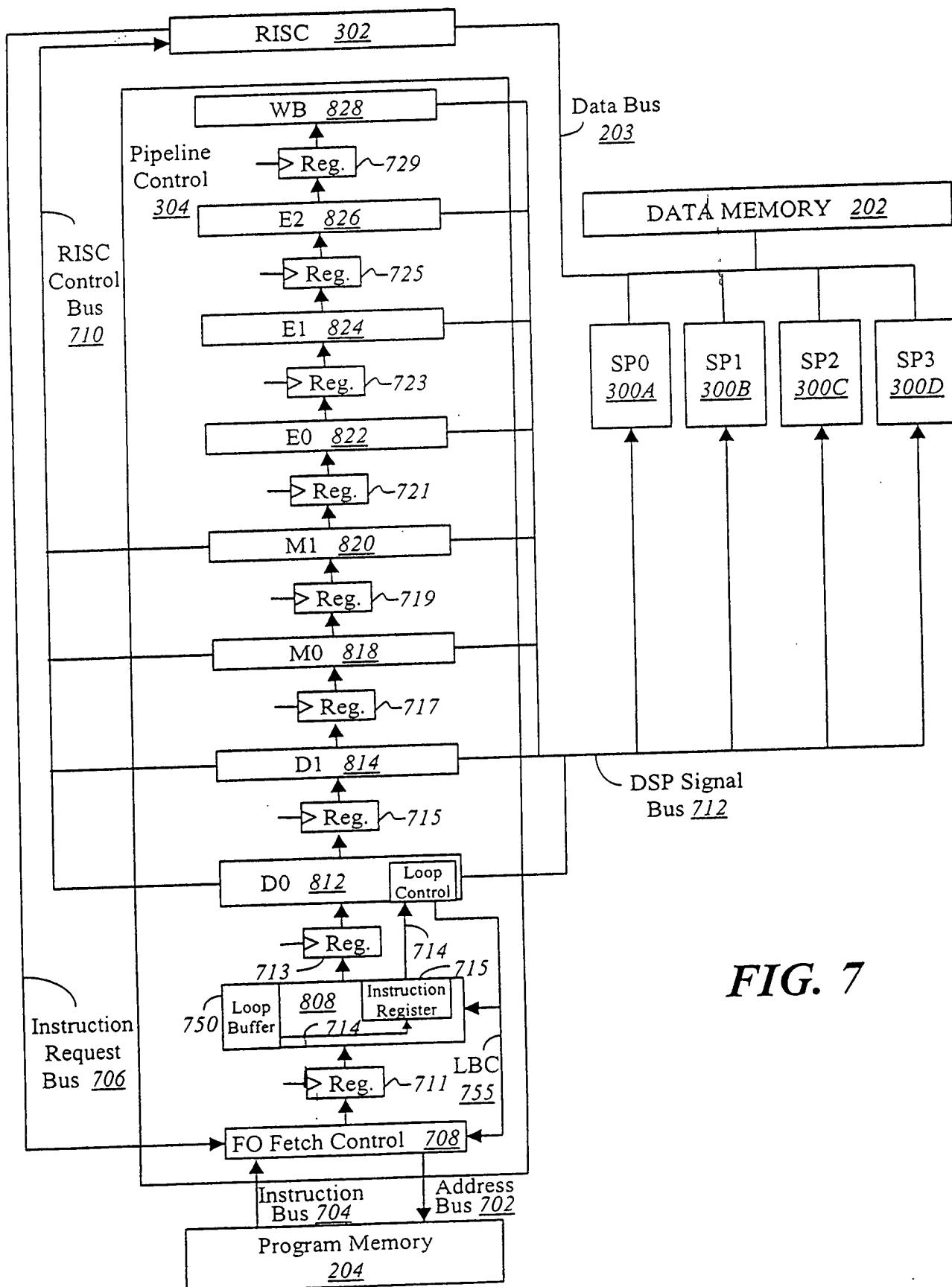


FIG. 7

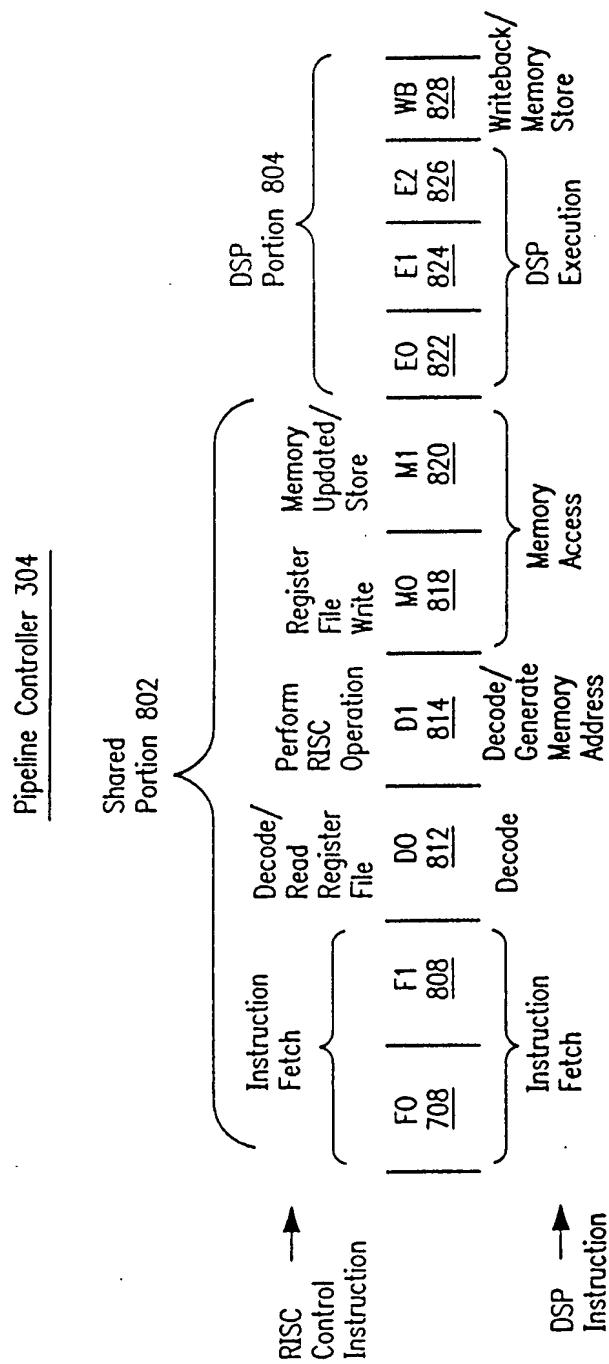


FIG. 8a

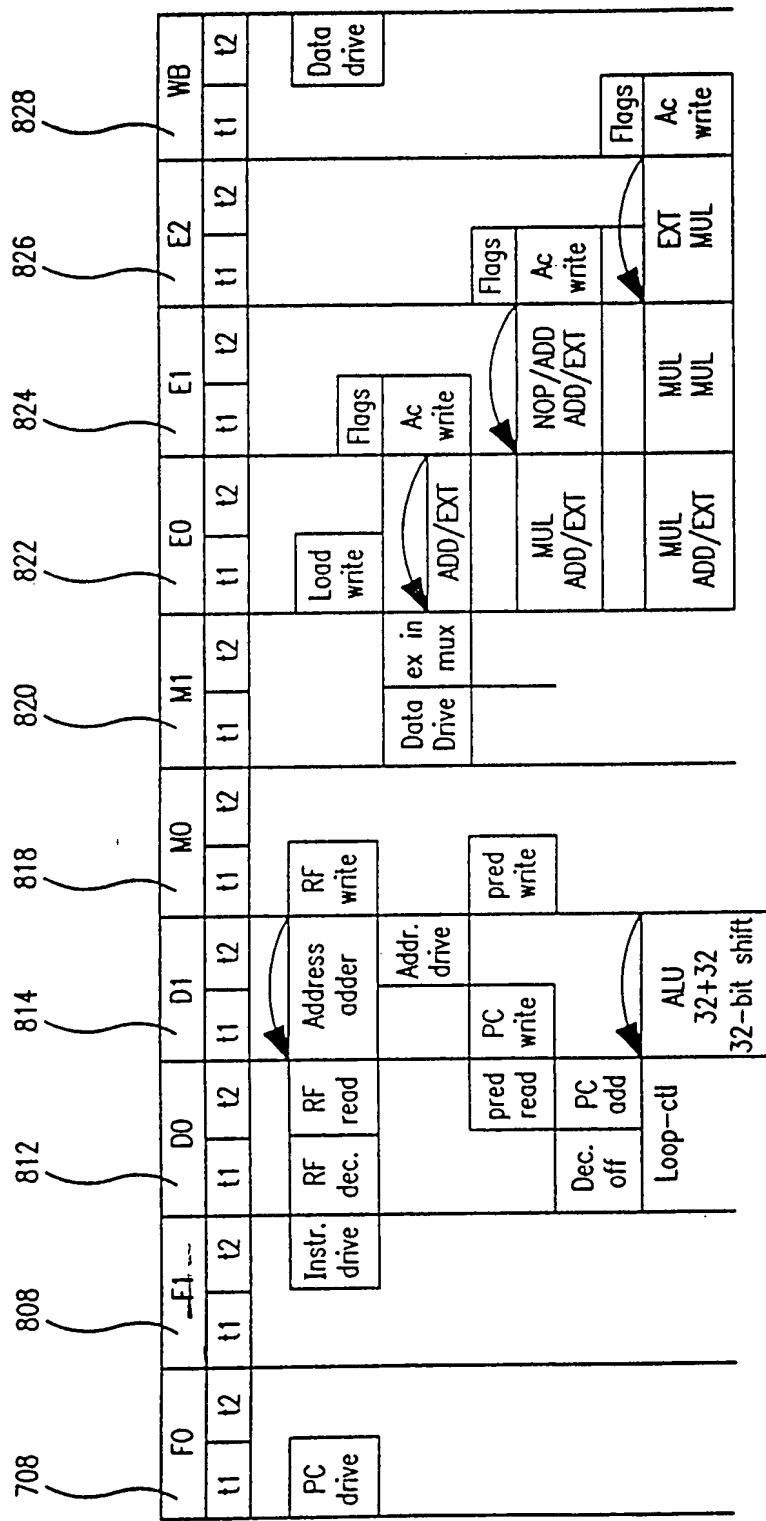
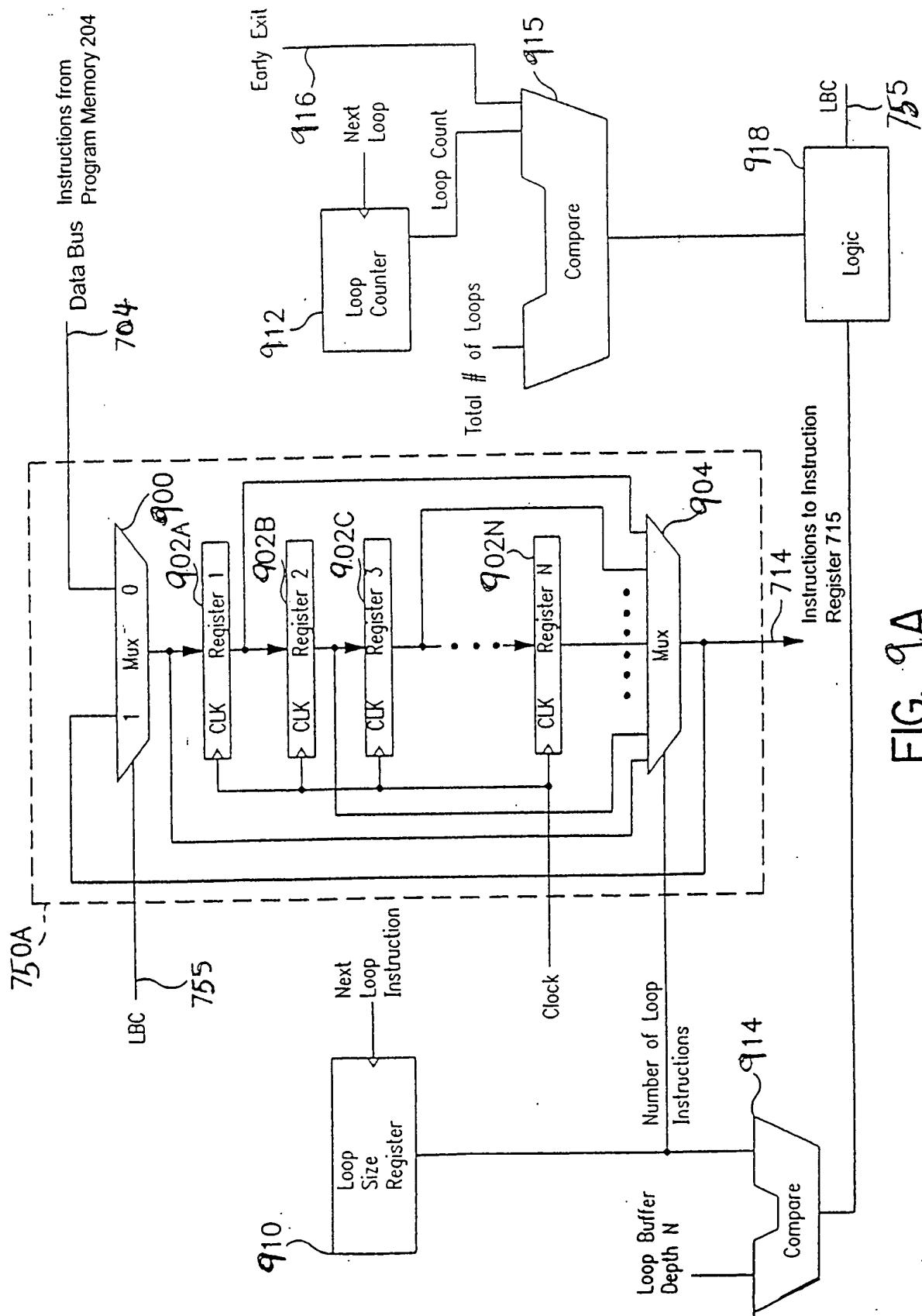


FIG. 8b



REPLACEMENT SHEET

**Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT**

1st Named Inventor: Ruban Kanapathippillai

Application No.: 10/649,067 Docket No.: 42P14037D

Sheet: 20/64

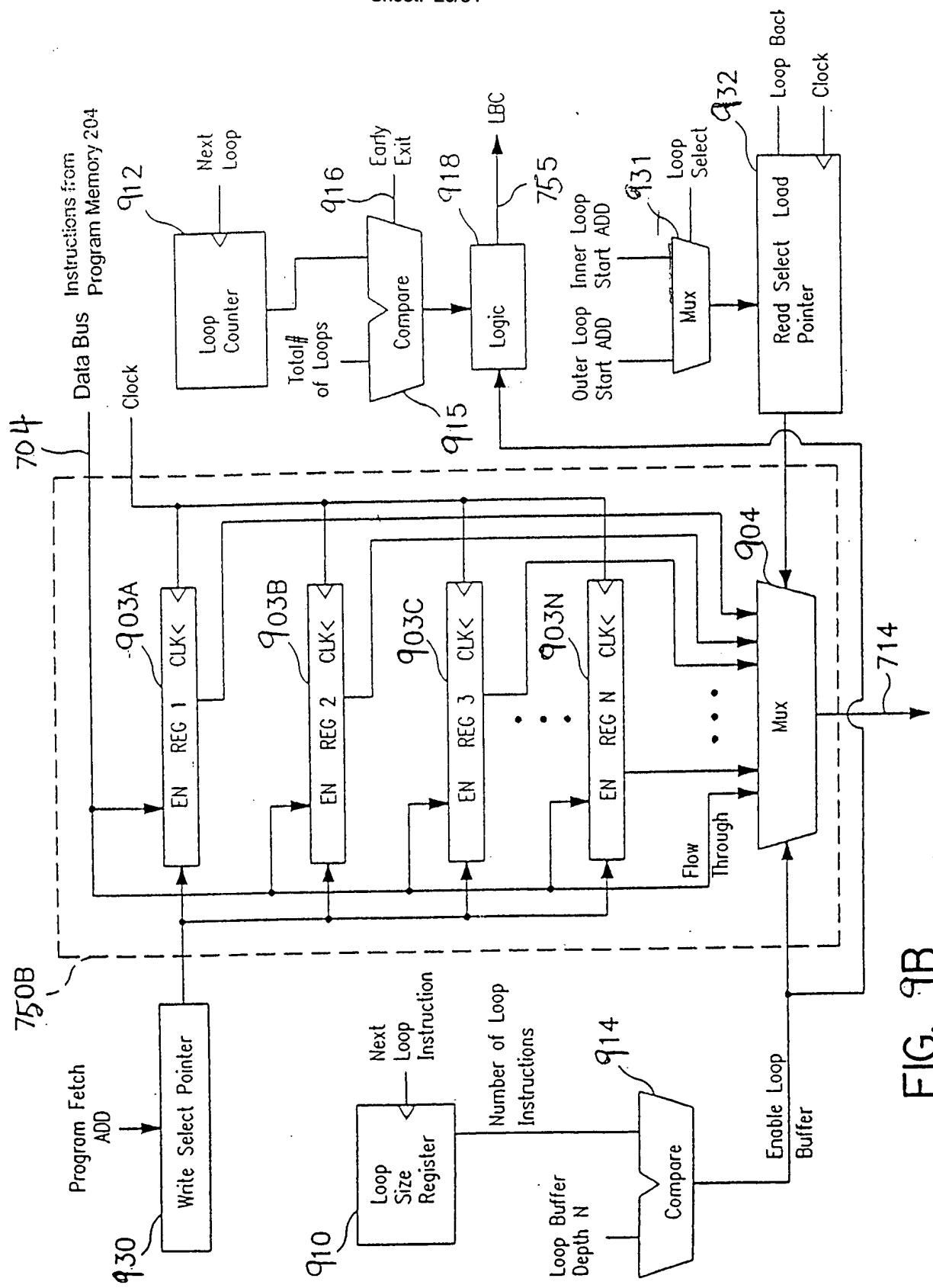


FIG. 9B

Instructions to Instruction
Register 715

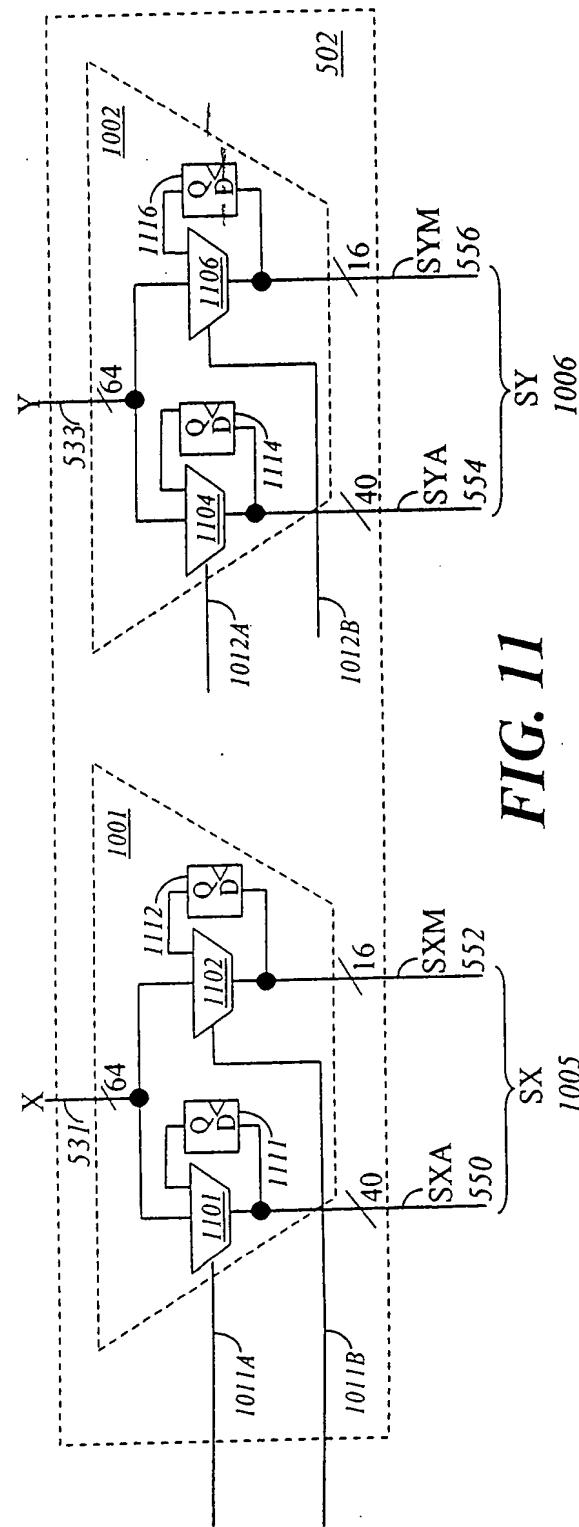
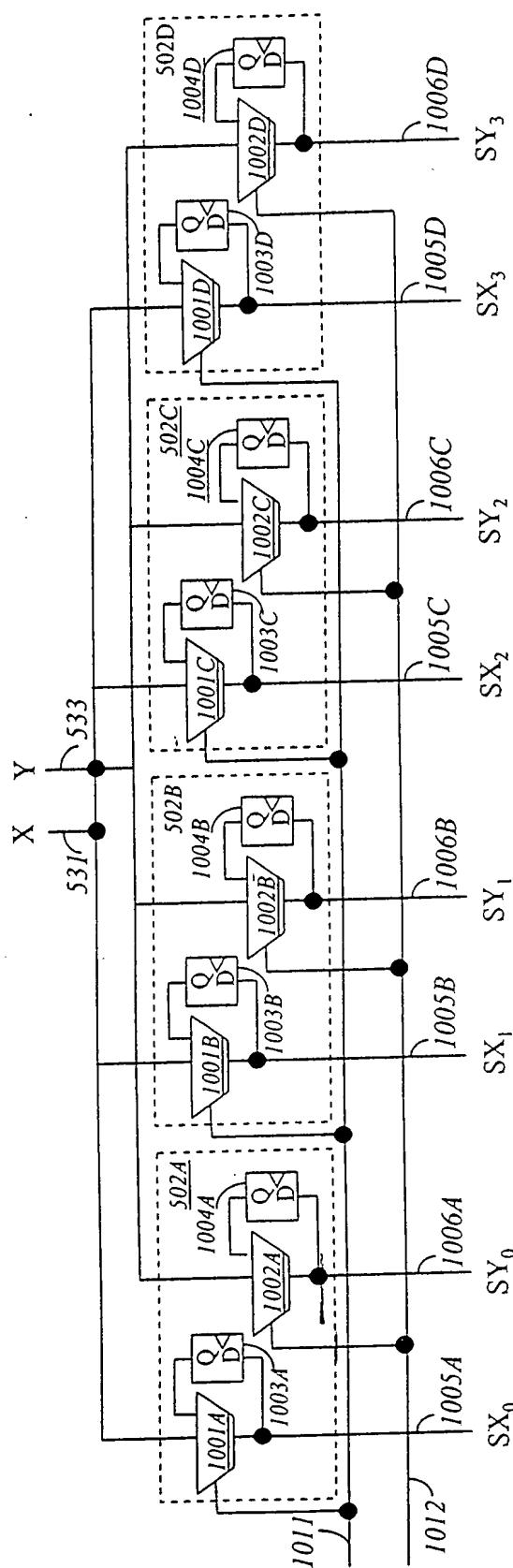


FIG. 12A

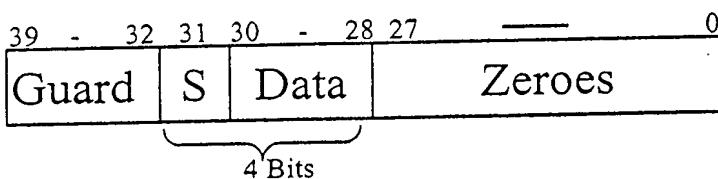
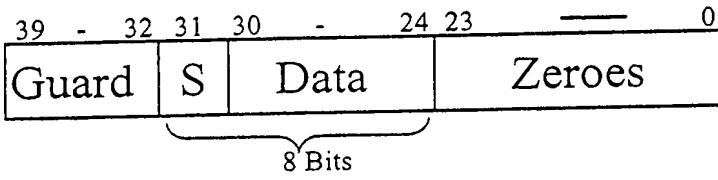
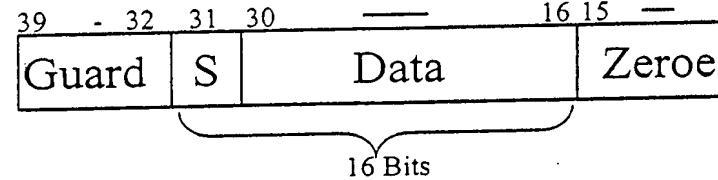
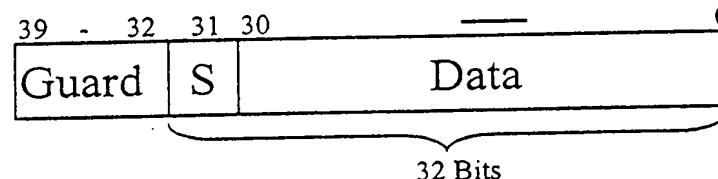
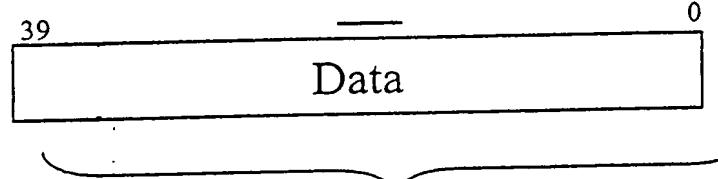
<u>Data Type</u>	<u>SP Configuration</u>
$1 \times 4 \text{ R}$	
$1 \times 8 \text{ R}$	
$1 \times 16 \text{ R}$	
$1 \times 32 \text{ R}$	
$1 \times 40 \text{ R}$	
SXA 550 or SYA 554	

FIG. 12B

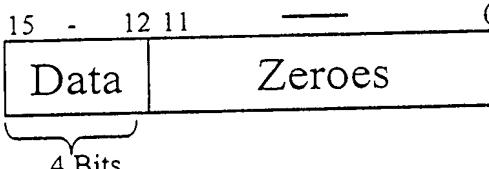
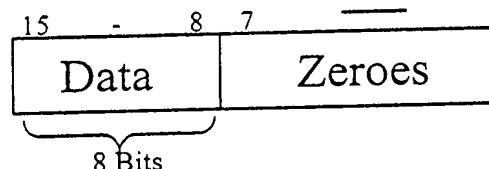
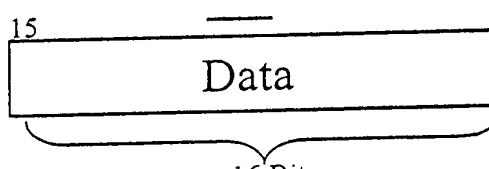
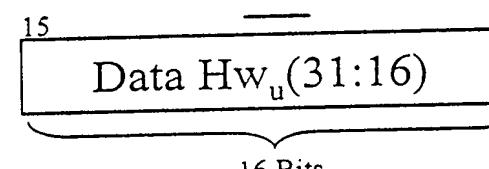
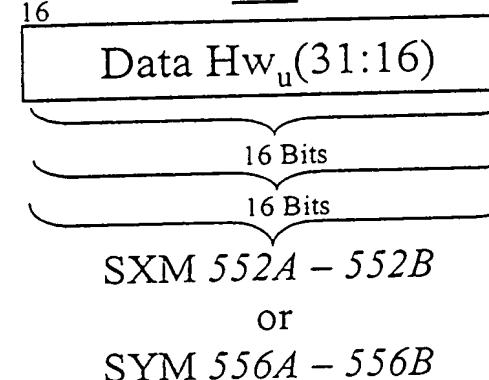
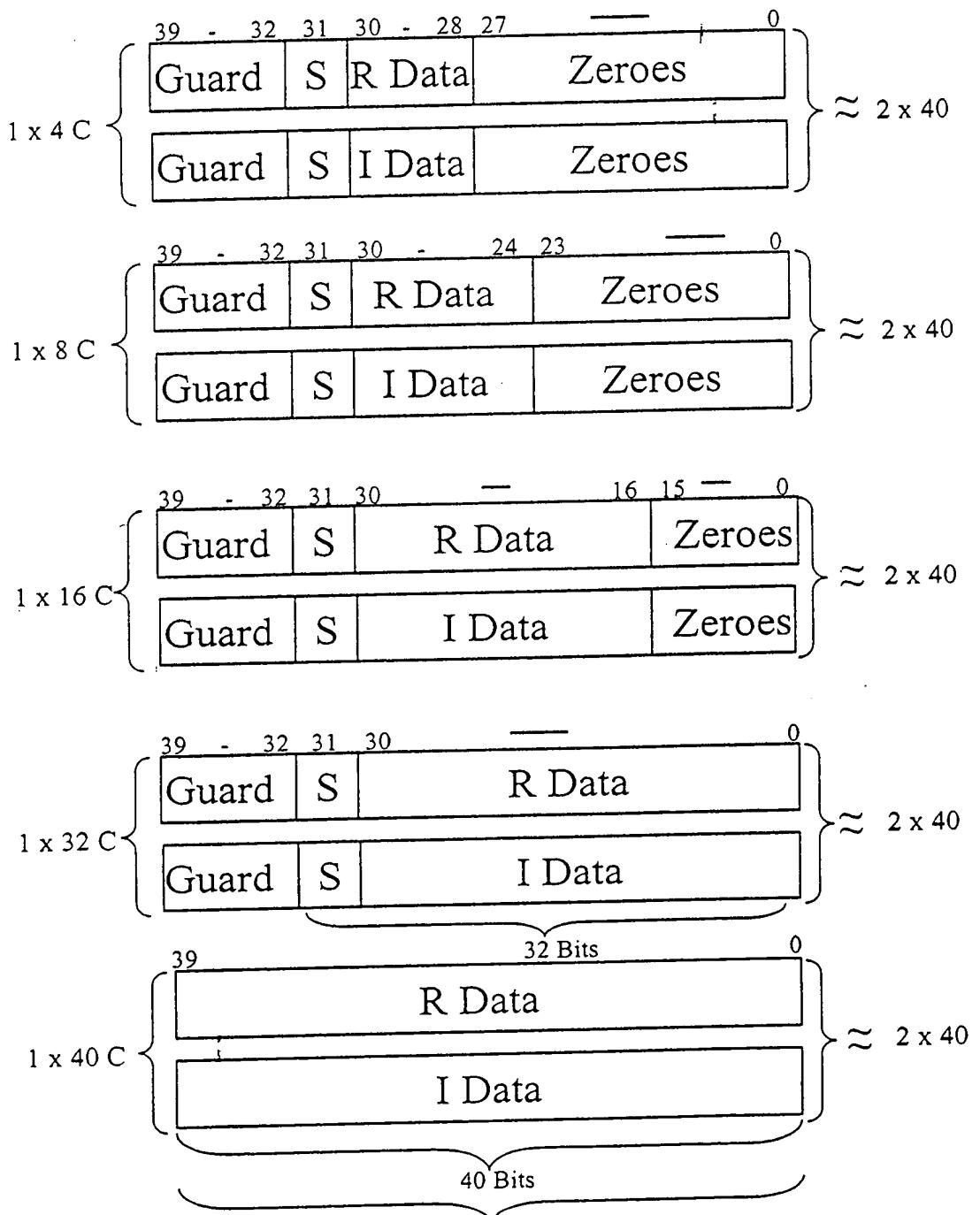
<u>Data Type</u>	<u>SP Configuration</u>
1 x 4 R	
1 x 8 R	
1 x 16 R	
1 x 32 R	
1 x 40 R	 <p style="text-align: center;">SXM 552A - 552B or SYM 556A - 556B</p>

FIG. 12C

Data Type

SP Configuration

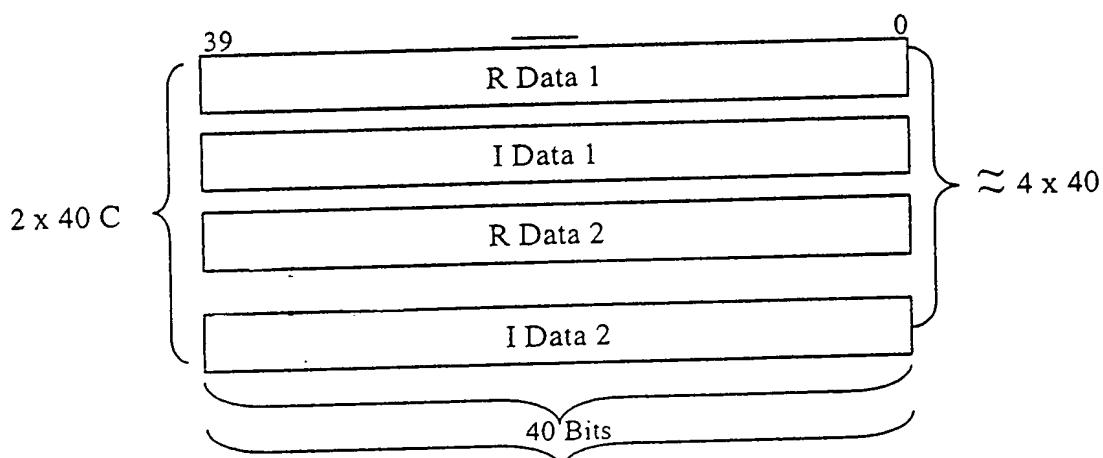
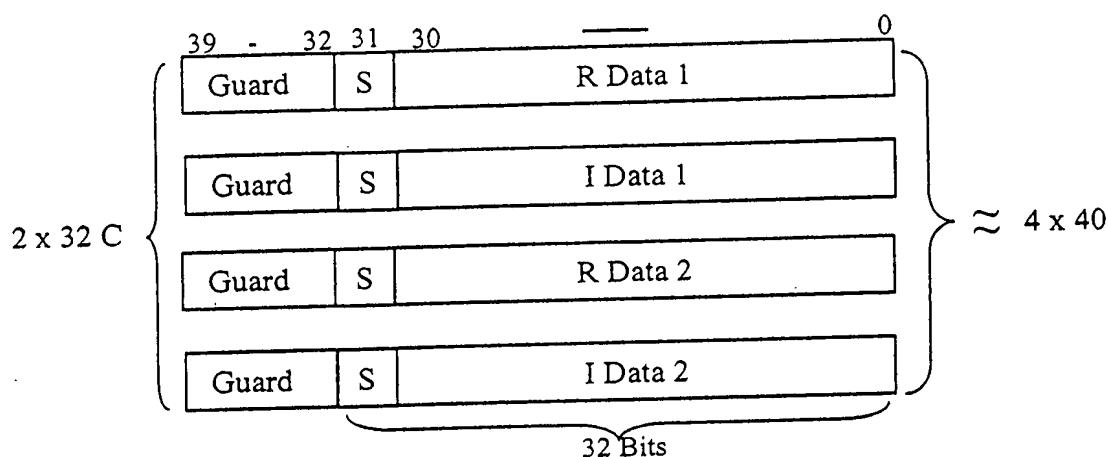
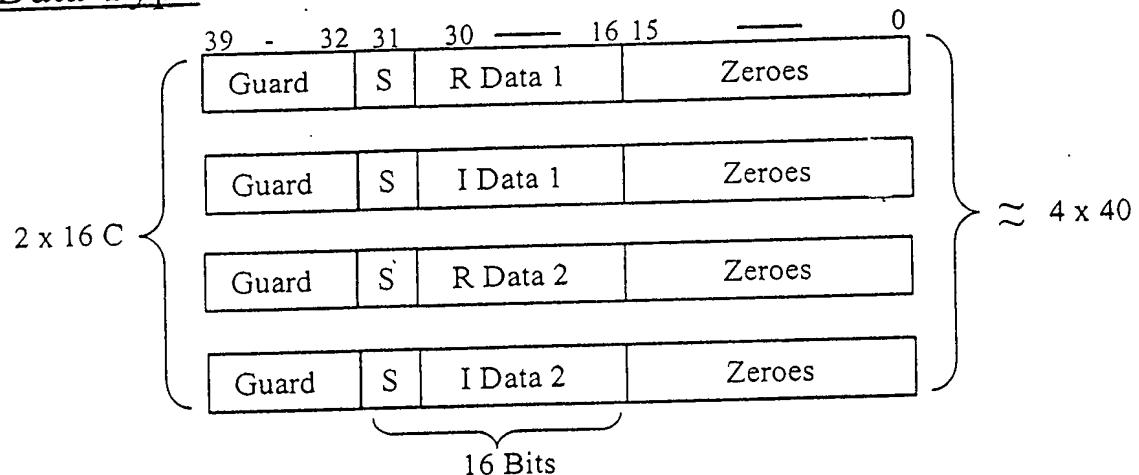


SXA 550A and SXA 550B
 or
 SYA 554A and SYA 554B

FIG. 12D

Data Type

SP Configuration



SXA 550A, SXA 550B, SXA 550C, and SXA 550D

or

SYA 554A, SYA 554B, SYA 554C, and SYA 554D

FIG. 12E

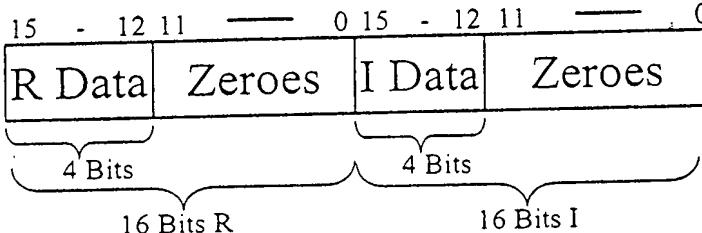
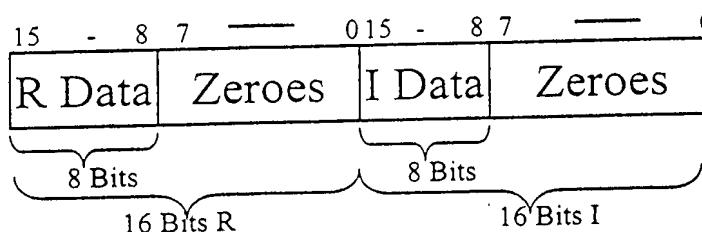
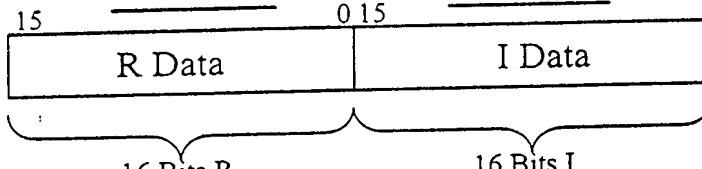
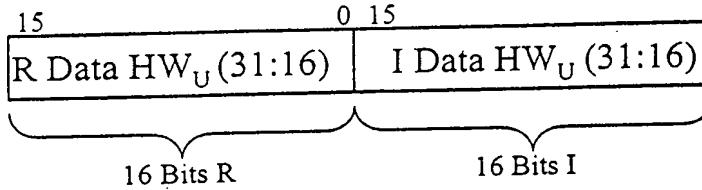
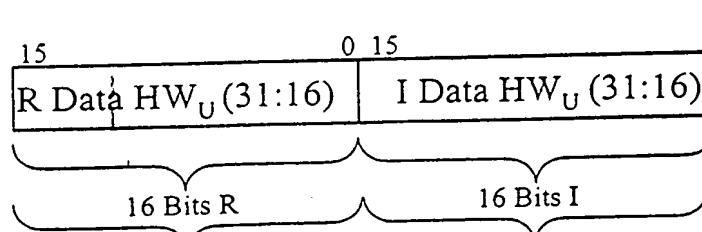
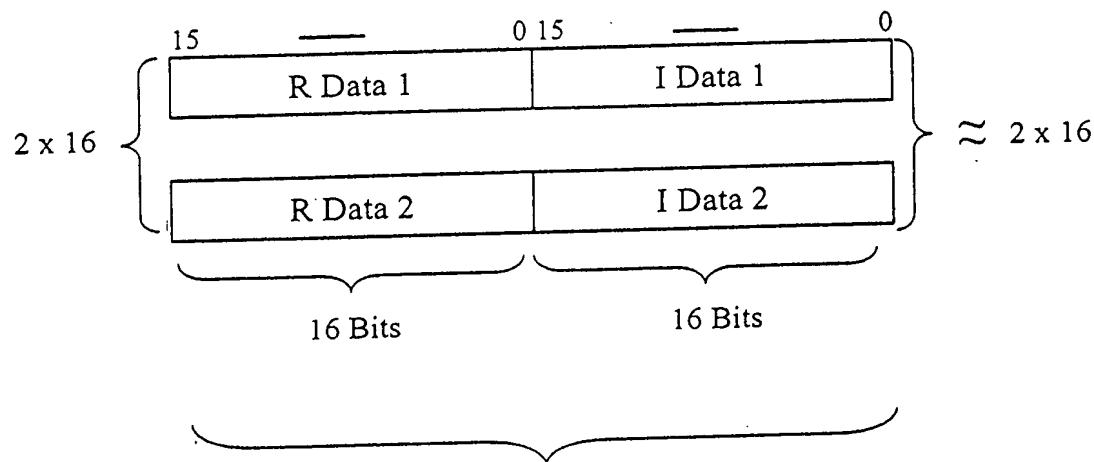
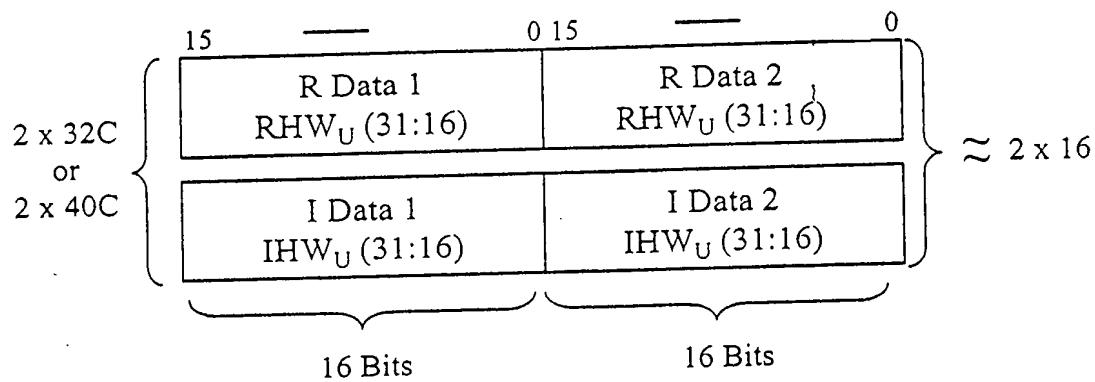
<u>Data Type</u>	<u>SP Configuration</u>
1 x 4 C	$\approx 2 \times 16$
	
1 x 8 C	$\approx 2 \times 16$
	
1 x 16 C	$\approx 2 \times 16$
	
1 x 32 C	$\approx 2 \times 16$
	
1 x 40 C	$\approx 2 \times 16$
	
SXM 552A and SXM 552B or SYM 556A and SYM 556B	

FIG. 12F

Data Type SP Configuration



SXM 552A, SXM 552B, SXM 552C, and SXM 552D
 or
 SYM 556A, SYM 556B, SYM 556C, and SYM 556D

Operand 1 Data Type: $N_1 \times S_1 R$
Operand 2 Data Type: $N_2 \times S_2 R$
Type Matching R: $\text{Max } (N_1 \text{ or } N_2) \times \text{Max } (S_1 \text{ or } S_2) R$

Fig. 13A

Operand 1 Data Type: $N_1 \times S_1 C$
Operand 2 Data Type: $N_2 \times S_2 C$
Type Matching C: $\text{Max } (N_1 \text{ or } N_2) \times \text{Max } (S_1 \text{ or } S_2) C$

Fig. 13B

Operand 1 Data Type: $N_1 \times S_1 R$
Operand 2 Data Type: $N_2 \times S_2 C$
Type Matching R+C: $\text{Max } (N_1 \text{ or } N_2) \times \text{Max } (S_1 \text{ or } S_2) C$

Fig. 13C

REPLACEMENT SHEET

Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR

BUSES IN AN INTEGRATED CIRCUIT

1st Named Inventor: Ruban Kanapathippillai

Application No.: 10/649,067

Docket No.: 42P14037D2

Sheet: 29/64

	1x16 real	2x16 real	1x16 cmplx	4x16 real	2x16 cmplx	1x32 real	2x32 cmplx	1x32 real	4x32 cmplx	2x32 real	1x40 real	2x40 real	1x40 real	4x40 real	2x40 cmplx
1x16 real	1	2		2	4			2	4						
2x16 real	2	2													
1x16 cmplx			2												
4x16 real			4												
2x16 cmplx				4											
1x32 real					2										
2x32 real						4									
1x32 cmplx															
4x32 real															
2x32 cmplx															
1x40 real															
2x40 real															
1x40 real															
4x40 real															
2x40 real															

FIG. 14

	1x16 real	2x16 real	1x16 cmplx	4x16 real	2x16 cmplx	1x32 real	2x32 real	1x32 cmplx	4x32 real	2x32 cmplx	1x40 real	2x40 real	1x40 real	4x40 real	2x40 cmplx
1x16 real	1	2		4		1	4		4		1	2		4	
2x16 real		2					2	2				2			
1x16 cmplx															
4x16 real	4														
2x16 cmplx															
1x32 real	1	2				1	2		4		1	2		4	
2x32 real	4	2					2	2				2			
1x32 cmplx															
4x32 real	4														
2x32 cmplx															
1x40 real	1						1					1			
2x40 real	2	2					2	2				2			
1x40 real															
4x40 real	4														
2x40 real															

FIG. 15A

1x16 real	2x16 real	1x16 cmplx	4x16 real	2x16 cmplx	1x32 real	2x32 cmplx	4x32 real	2x32 cmplx	1x40 real	2x40 real	1x40 real	4x40 real	2x40 cmplx
1x16 real	1 unit	2 unit	4 unit	4 unit	1 unit	2 unit	4 unit	4 unit	1 unit	2 unit	2 unit	4 unit	4 unit
2x16 real	2 unit	2 unit			2 unit	2 unit				2 unit			
1x16 cmplx	2 unit									2 unit	2 unit		
4x16 real	4 unit												
2x16 cmplx	4 unit												
1x32 real	1 unit	2 unit			1 unit	2 unit	2 unit	4 unit		4 unit	1 unit	2 unit	4 unit
2x32 real	2 unit	2 unit			2 unit	2 unit					2 unit	2 unit	
1x32 cmplx	2 unit				2 unit	2 unit					2 unit	2 unit	
4x32 real	4 unit				4 unit	4 unit					4 unit	4 unit	
2x32 cmplx	4 unit				4 unit								
1x40 real	1 unit	2 unit			1 unit		2 unit	4 unit		1 unit	2 unit	4 unit	
2x40 real	2 unit	2 unit			2 unit	2 unit				2 unit	2 unit		
1x40 real	2 unit				2 unit		2 unit				2 unit		
4x40 real	4 unit				4 unit								
2x40 real	4 unit				4 unit								

FIG. 15B

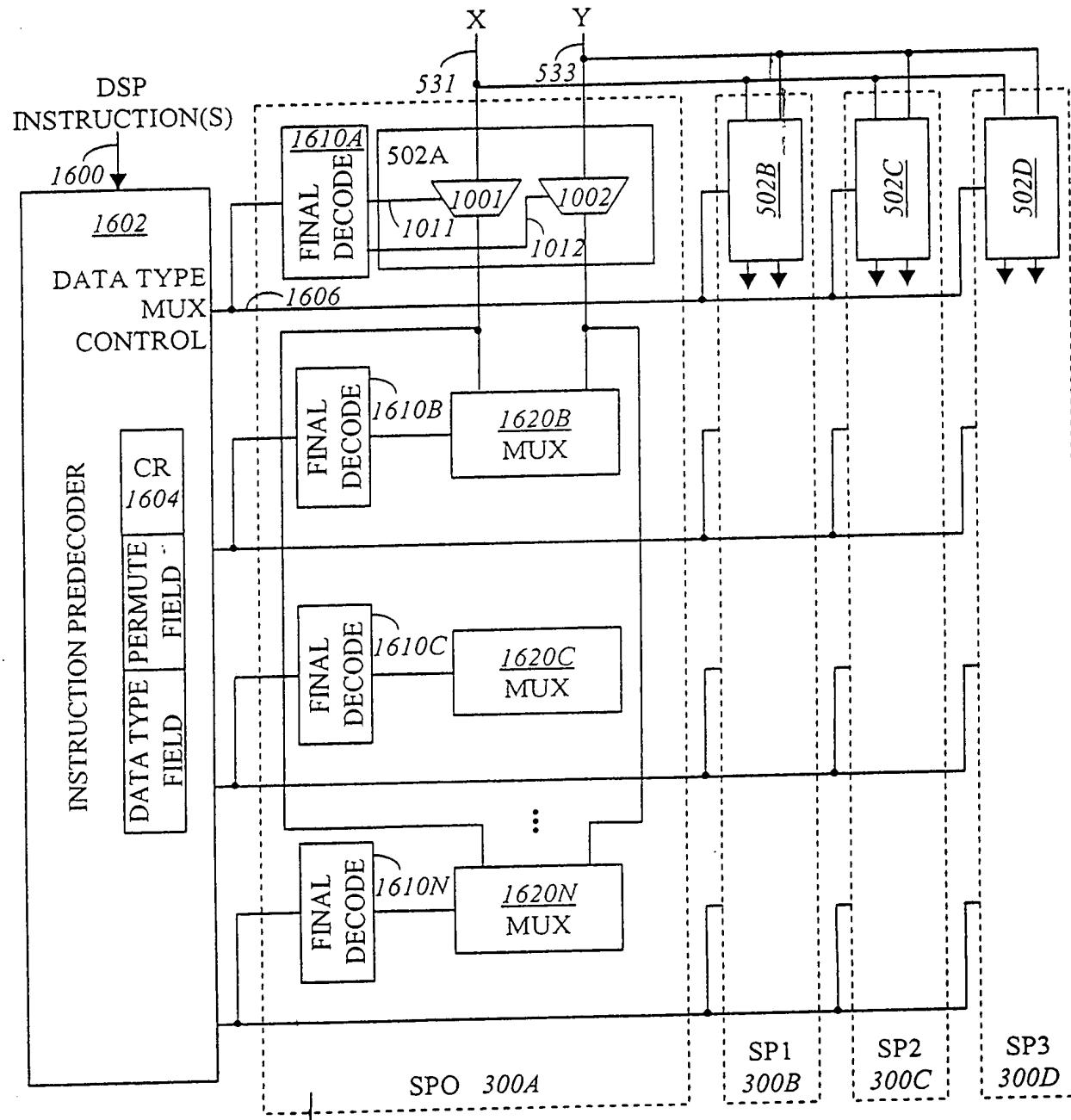


FIG. 16

Data Type: N x S(R/C)

FIG. 17

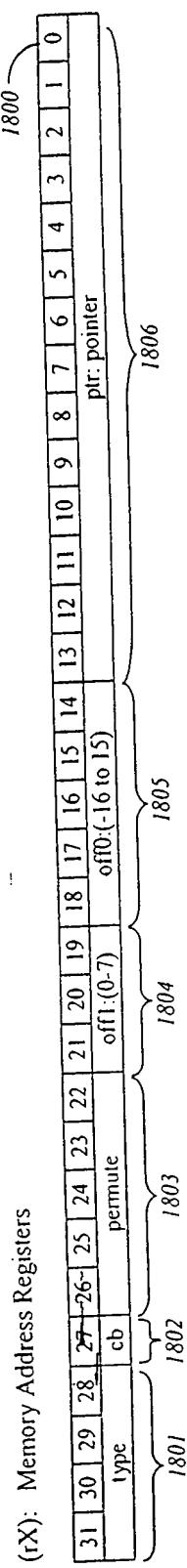


FIG. 18

Data Type 1801

0000:	1x16 real
0001:	2x16 real
0010:	1x16 complex
0011:	4x16 real
0100:	1x32 real
0101:	2x32 real
0110:	1x32 complex
0111:	2x16 complex
1000:	4x32 real
1001:	2x32 complex
1010:	1x40 real
1011:	2x40 real
1100:	1x40 complex
1101:	4x40 real (only for local add unit operations)
1110:	2x40 complex (only for local add unit operations)
1111:	Reserved

FIG. 19

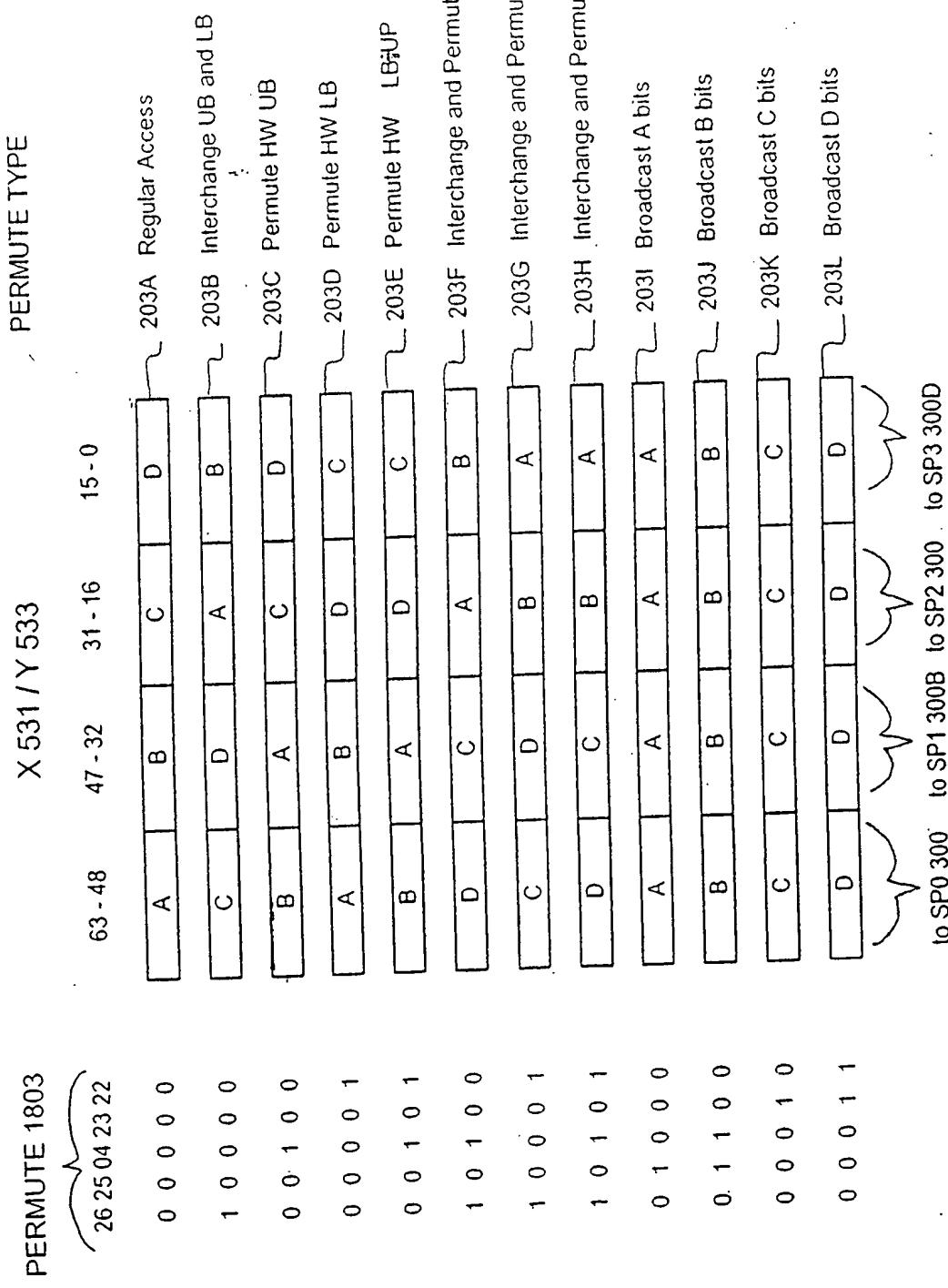
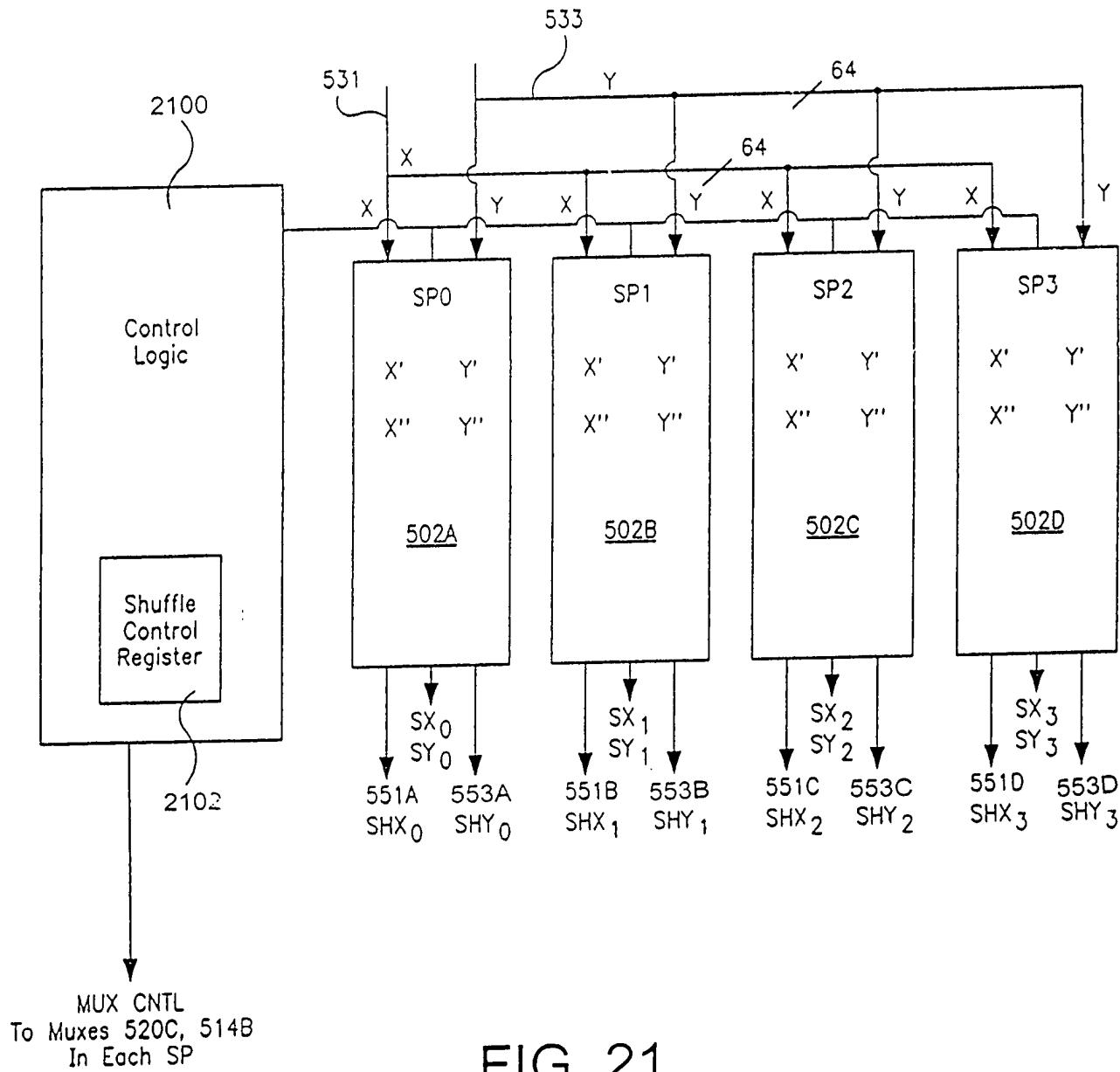


FIG. 20



$X' = [SX_{10}, SX_{11}, SX_{12}, SX_{13}]$ e.g. $[X_0, X_1, X_2, X_3]$
 $X'' = [SX_{20}, SX_{21}, SX_{22}, SX_{23}]$ e.g. $[X_4, X_5, X_6, X_7]$

Where SX_{ab} : S=Source; a=delay; b= SP unit number(e.g. SP3,SP2, SP1, SP0; or termed U3,U2,U1,U0)

$Y' = [SY_{10}, SY_{11}, SY_{12}, SY_{13}]$
 $Y'' = [SY_{20}, SY_{21}, SY_{22}, SY_{23}]$

Where SY_{ab} : S=Source; a=delay; b= SP unit number(e.g. SP3,SP2,SP1, SP0; or termed U3,U1,U0)

FIG. 22A

FIR Filter

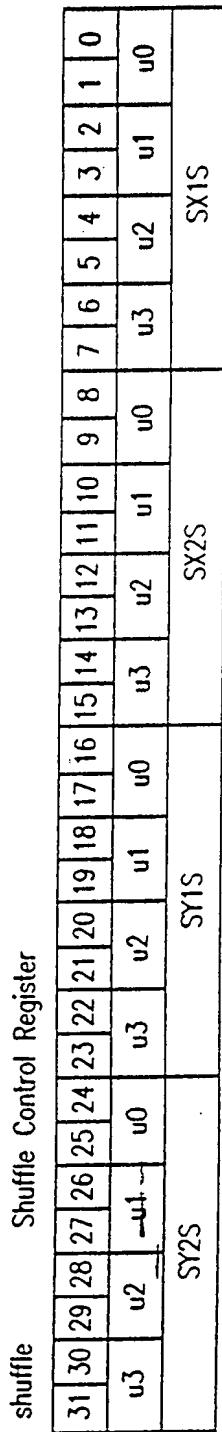
$$\begin{bmatrix} x_0 \\ x_1 \\ \vdots \\ x_N \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix} = x_0 y_0 + x_1 y_1 + \dots + x_N y_N$$

Primary Stage		Primary Stage Computations			
Cycle #		SP0	SP1	SP2	SP3
1		$x_0 y_0$	$x_1 y_1$	$x_2 y_2$	$x_3 y_3$
2		$x_4 y_4$	$x_5 y_5$	$x_6 y_6$	$x_7 y_7$
3		$x_8 y_8$	$x_9 y_9$	$x_{10} y_{10}$	$x_{11} y_{11}$
:					
N		$x_{N-3} y_{N-3}$	$x_{N-2} y_{N-2}$	$x_{N-1} y_{N-1}$	$x_N y_N$

Shadow Stage		Shadow Stage Computations			
Cycle #		SP0	SP1	SP2	SP3
1	No operation				
2	No operation				
3		$x_1 y_0$	$x_2 y_1$	$x_3 y_2$	$x_4 y_3$
4		$x_5 y_4$	$x_6 y_5$	$x_7 y_6$	$x_8 y_7$
:					
N+2		$x_{N-2} y_{N-3}$	$x_{N-1} y_{N-2}$	$x_N y_{N-1}$	$x_{N+1} y_N$

Subsequent Cycles					
Primary Stage			Shadow Stage		
Cycle #			Cycle #		
N+1		$\begin{bmatrix} x_2 \\ \vdots \\ x_{N+2} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$		N+3	$\begin{bmatrix} x_3 \\ \vdots \\ x_{N+3} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$
:				N+5	$\begin{bmatrix} x_5 \\ \vdots \\ x_{N+5} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$
N+4		$\begin{bmatrix} x_4 \\ \vdots \\ x_{N+4} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$		N+6	$\begin{bmatrix} x_6 \\ \vdots \\ x_{N+6} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$
:				N+7	$\begin{bmatrix} x_7 \\ \vdots \\ x_{N+7} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$

FIG. 22B



Units are connected to their nearest neighbors for shuffling the sources using the following bit diagram:

00	Unit N+1, SX1=X'	(right)
01	Unit N+1, SX2=X''	(right)
10	Unit N-1, SX1=X'	(left)
11	Unit N-1, SX2=X''	(left)

For example to shift the sources to the left by one:

3	2	1	0	From
2	1	0	3	Into

The bits should be 10101010 (AA)

FIG. 22C

REPLACEMENT SHEET

REPLACEMENT SHEET
Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR

BUSES IN AN INTEGRATED CIRCUIT

1st Named Inventor: Ruban Kanapathippillai

Application No.: 10/649,067

Docket No.: 42P14037D2

Sheet: 39/64

FIG. 23A

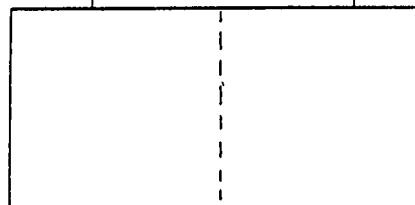


FIG. 23B

FIG. 23

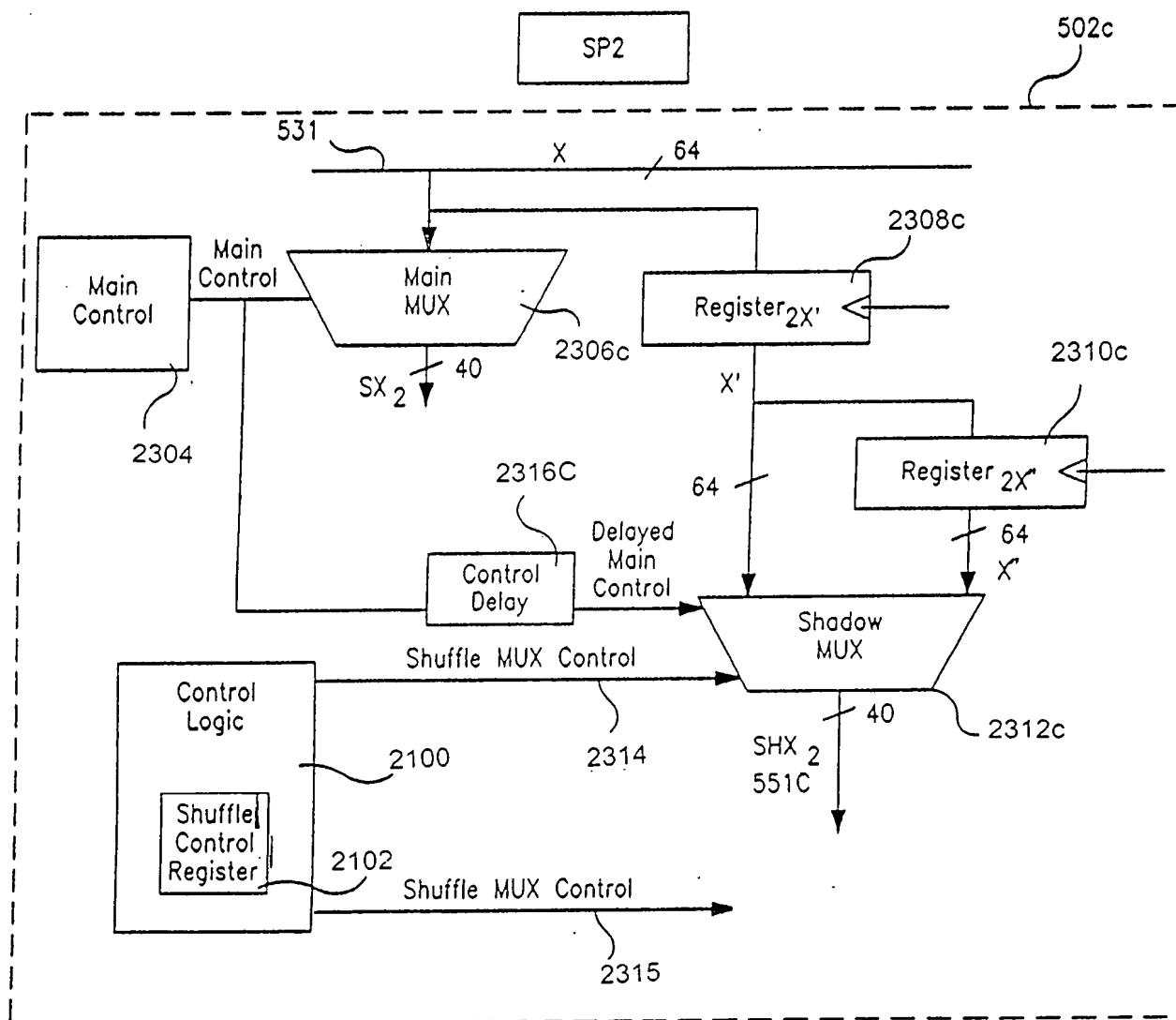


FIG. 23A

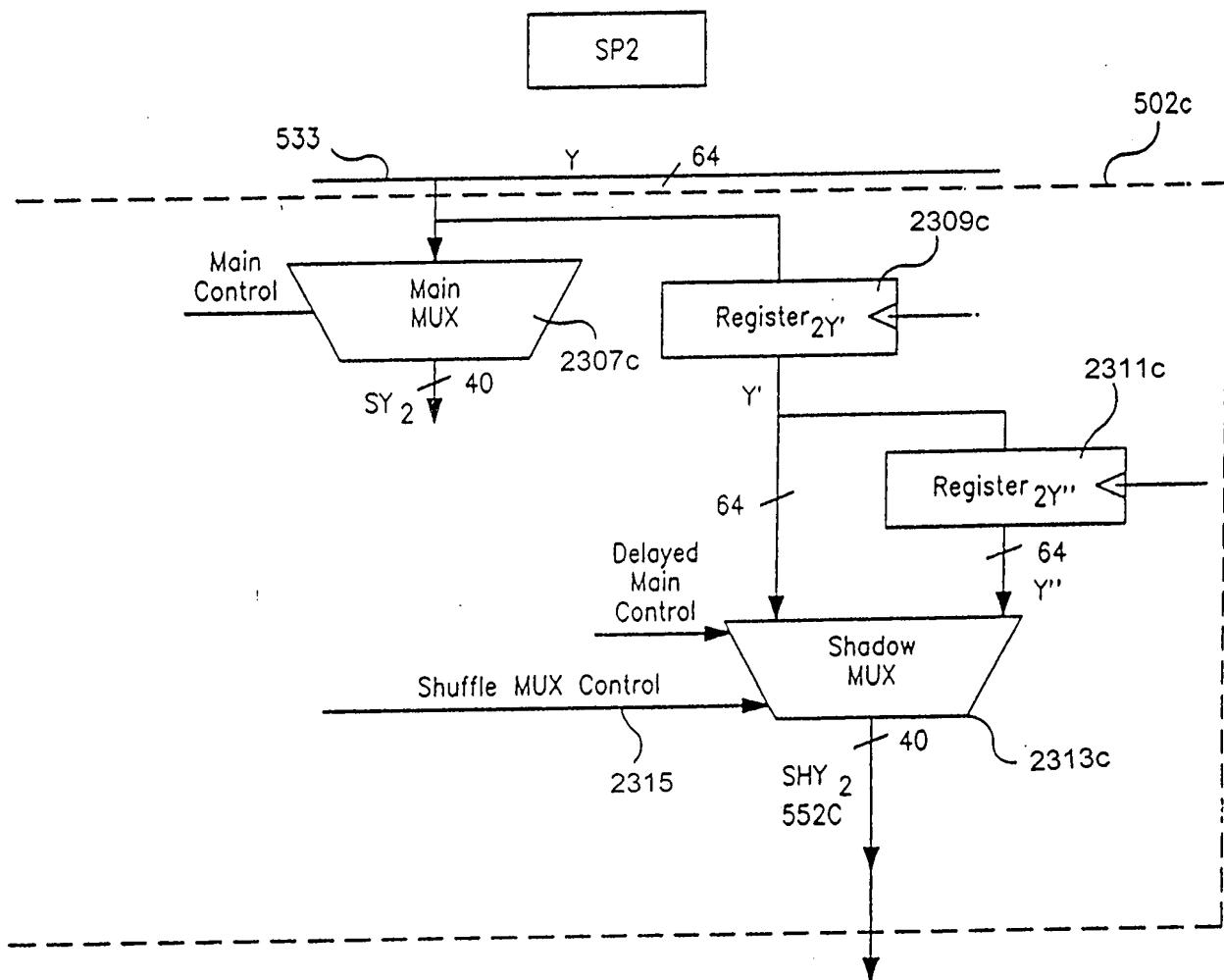


FIG. 23B

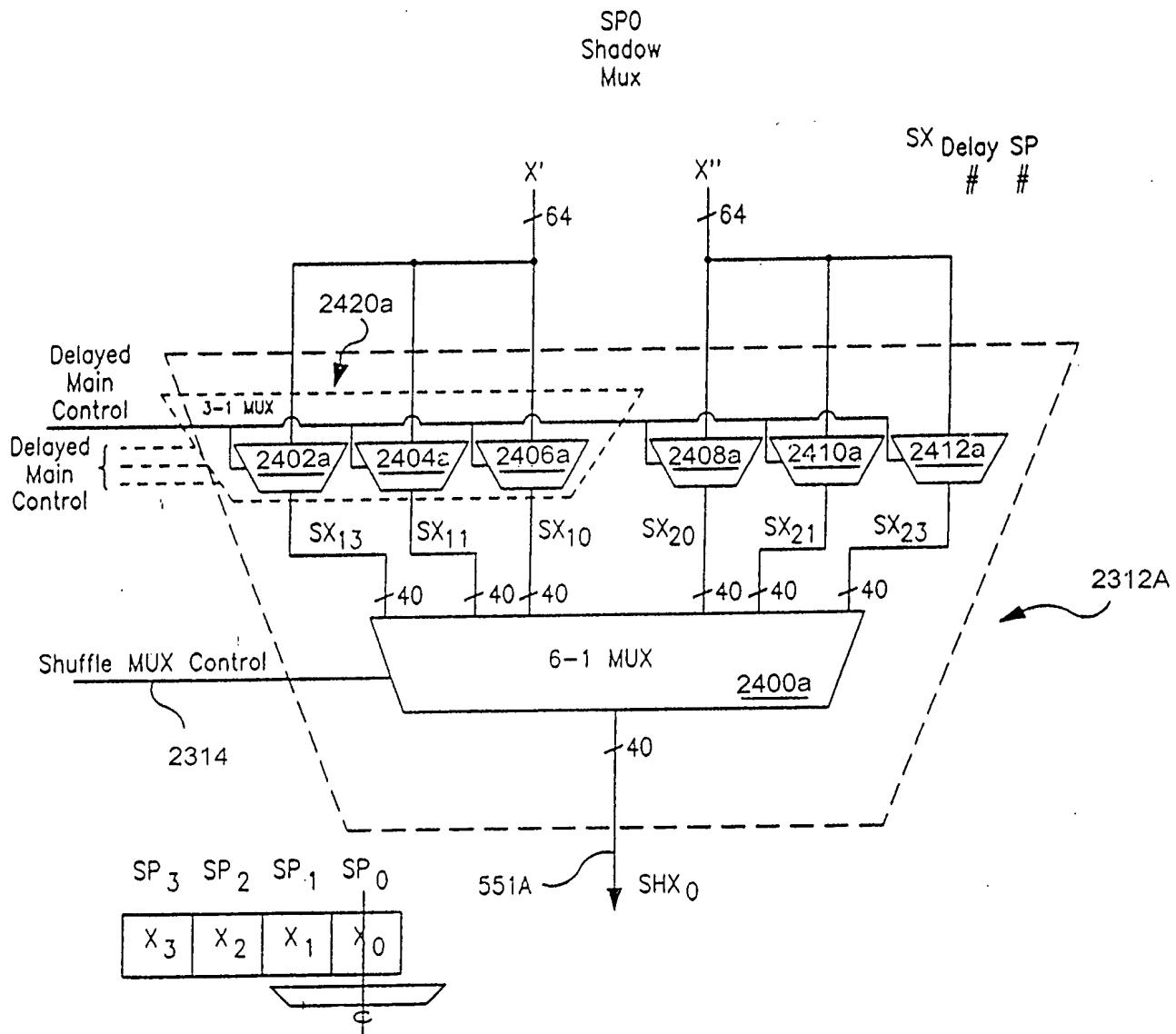
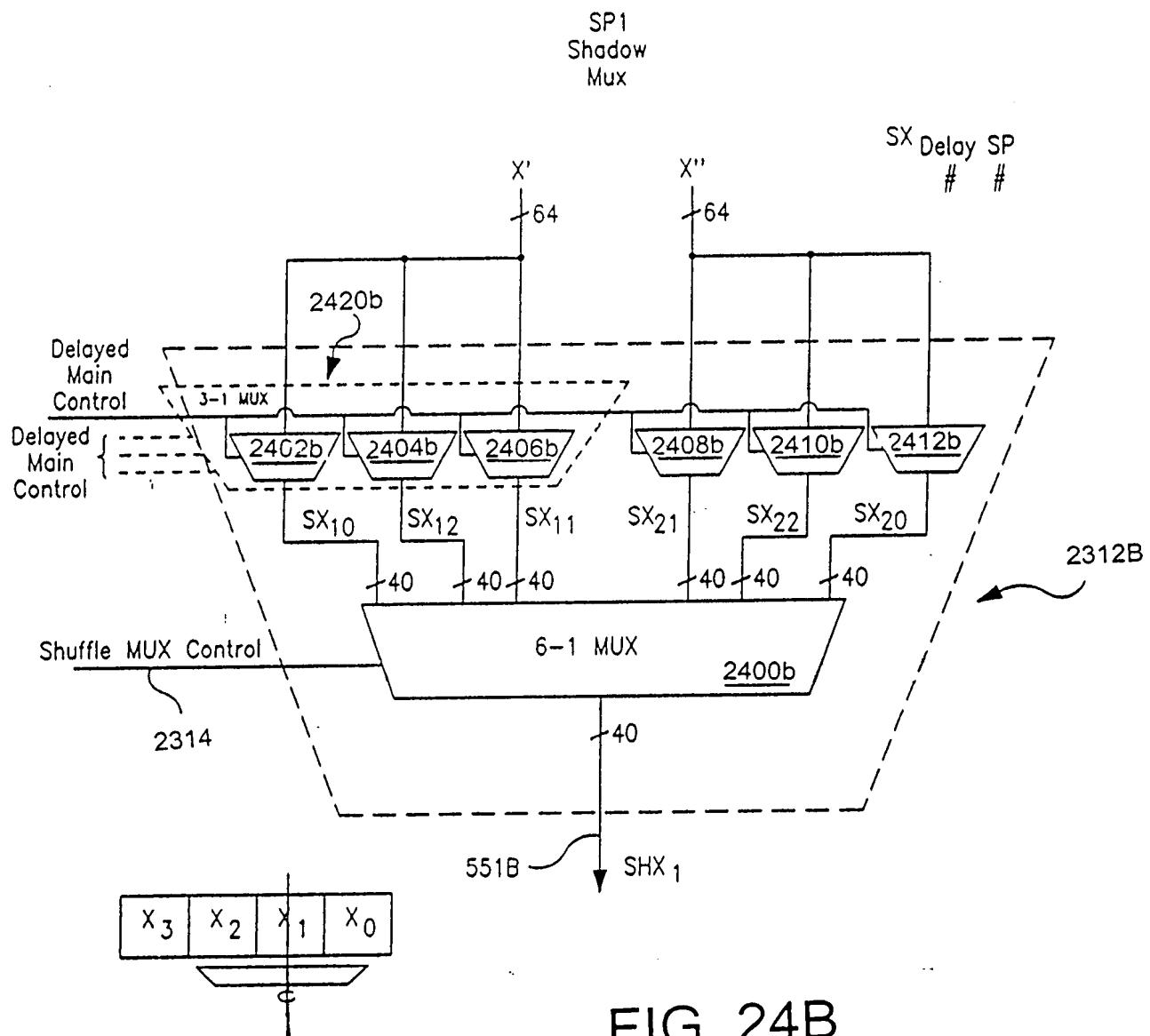


FIG. 24A

$X_0 = SX_{10}, SX_{20}$

$X_1 = SX_{11}, SX_{21}$

$X_3 = SX_{13}, SX_{23}$



$X_1 = SX_{11}, SX_{21}$
 $X_2 = SX_{12}, SX_{22}$
 $X_0 = SX_{10}, SX_{20}$

FIG. 24B

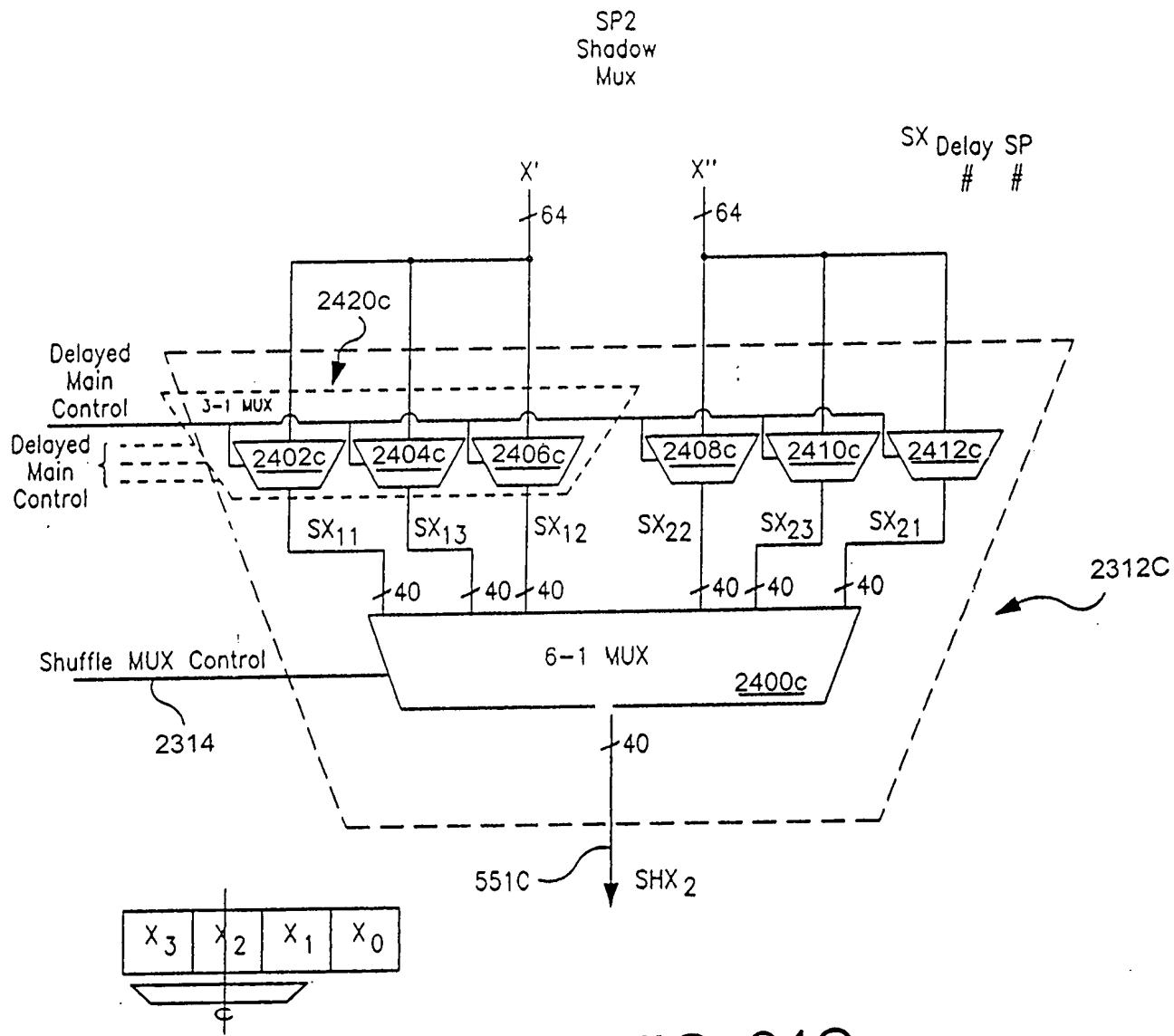
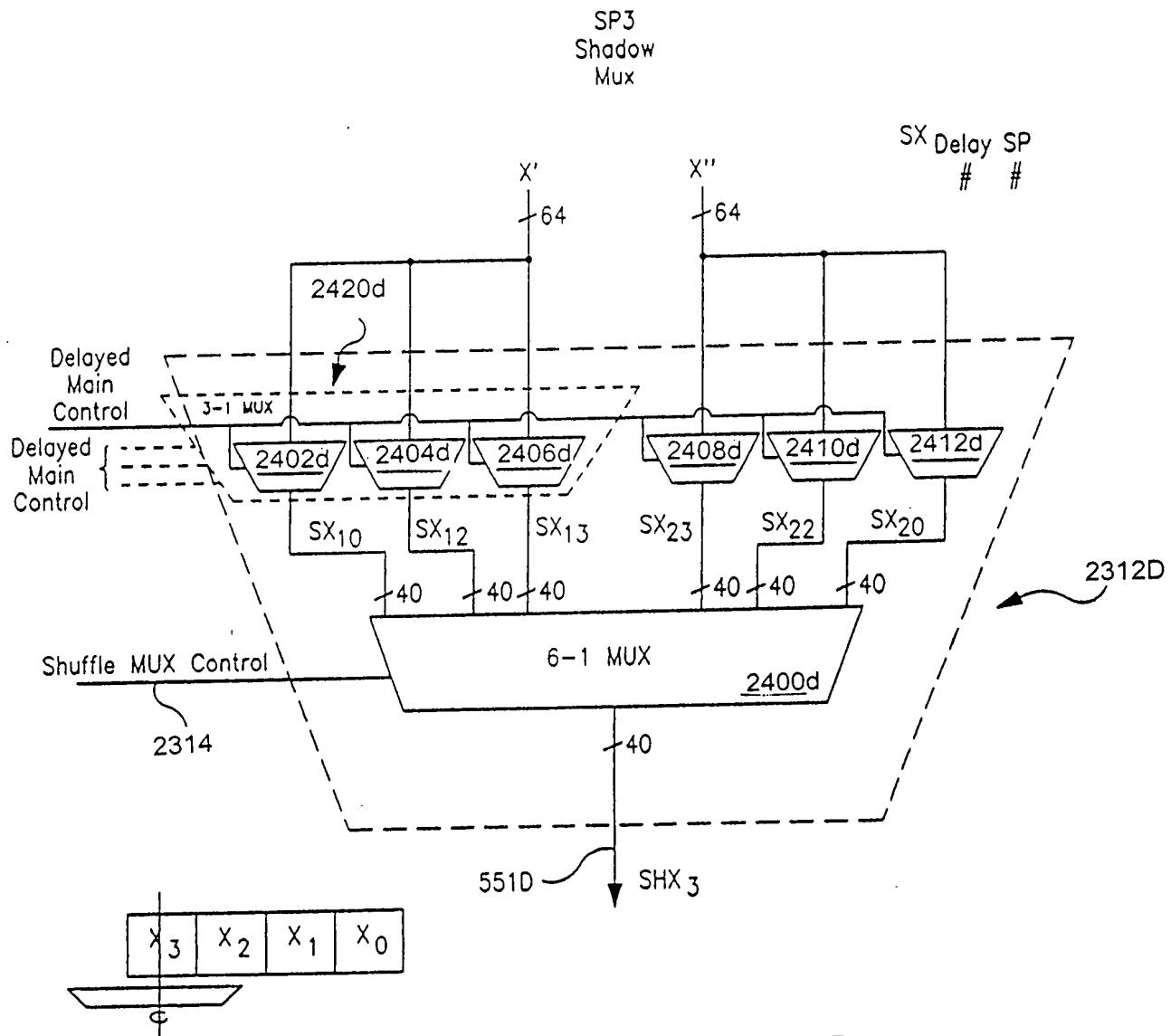


FIG. 24C

$X_2 = SX_{12}, SX_{22}$
 $X_3 = SX_{13}, SX_{23}$
 $X_1 = SX_{11}, SX_{21}$



$X_3 = SX_{13}, SX_{23}$
 $X_0 = SX_{10}, SX_{20}$
 $X_2 = SX_{12}, SX_{22}$

FIG. 24D

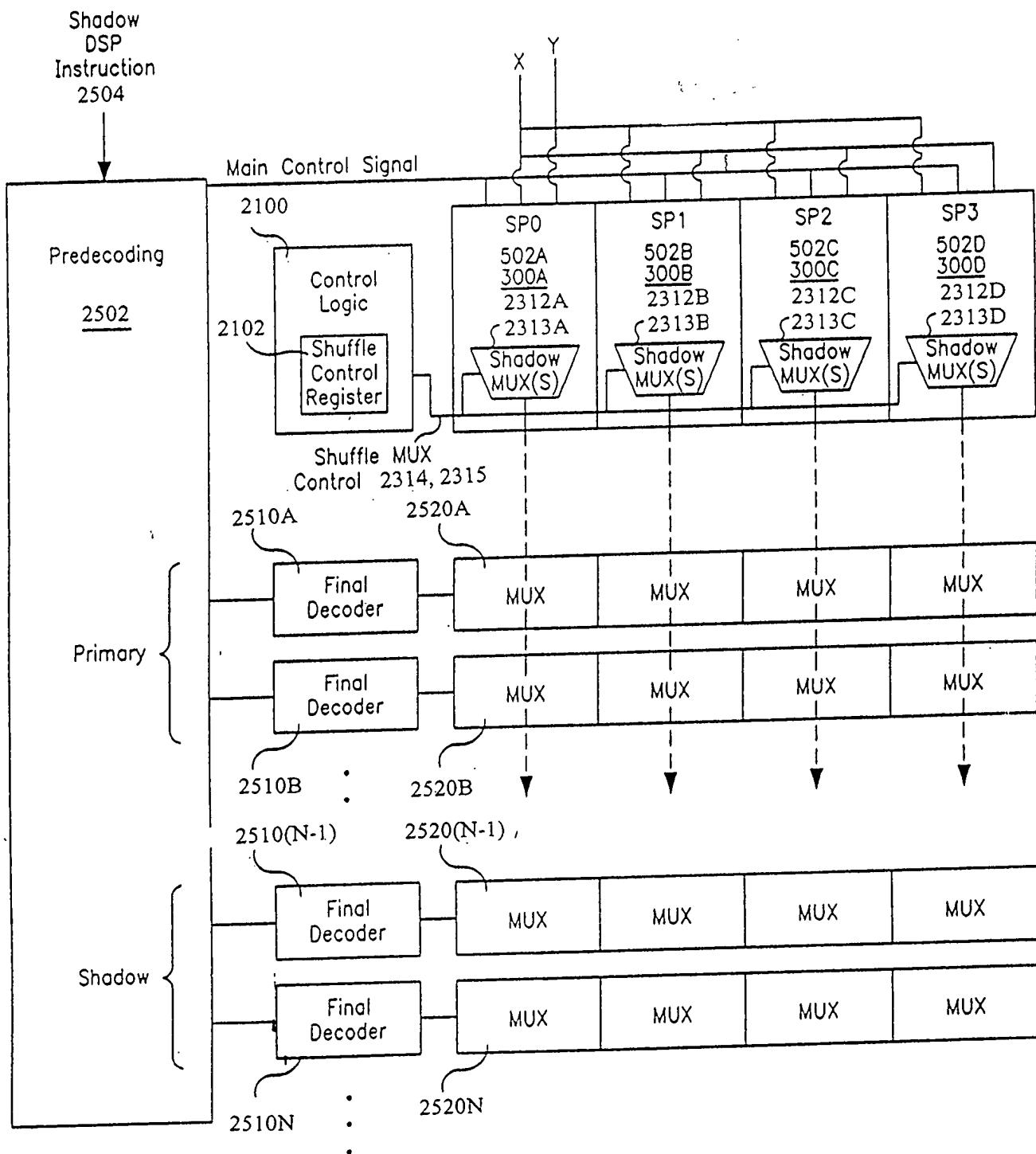


FIG. 25

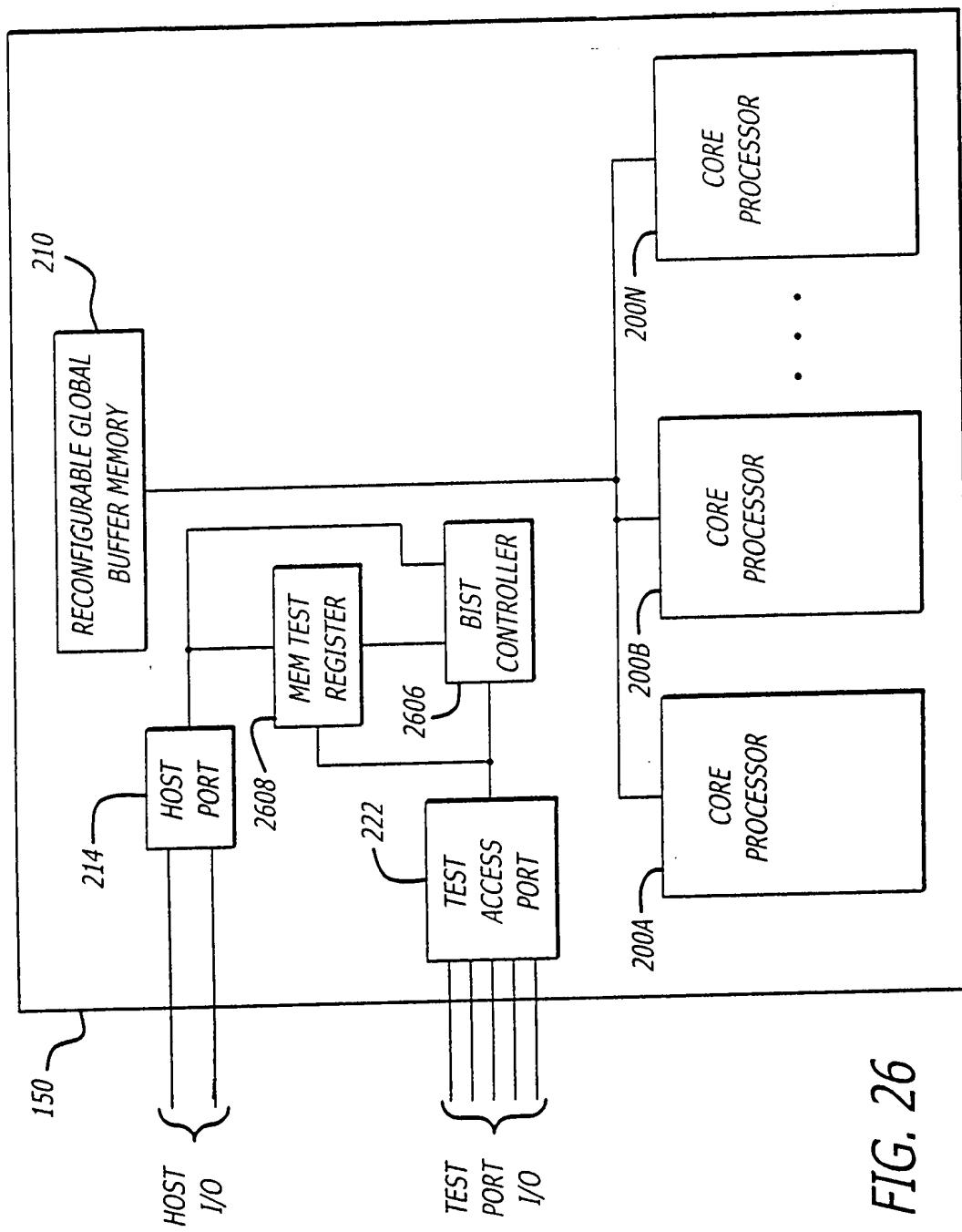


FIG. 26

REPLACEMENT SHEET

**Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT**

1st Named Inventor: Ruban Kanapathippillai

Application No.: 10/649,067 Docket No.: 42P14037D

Sheet: 47/64

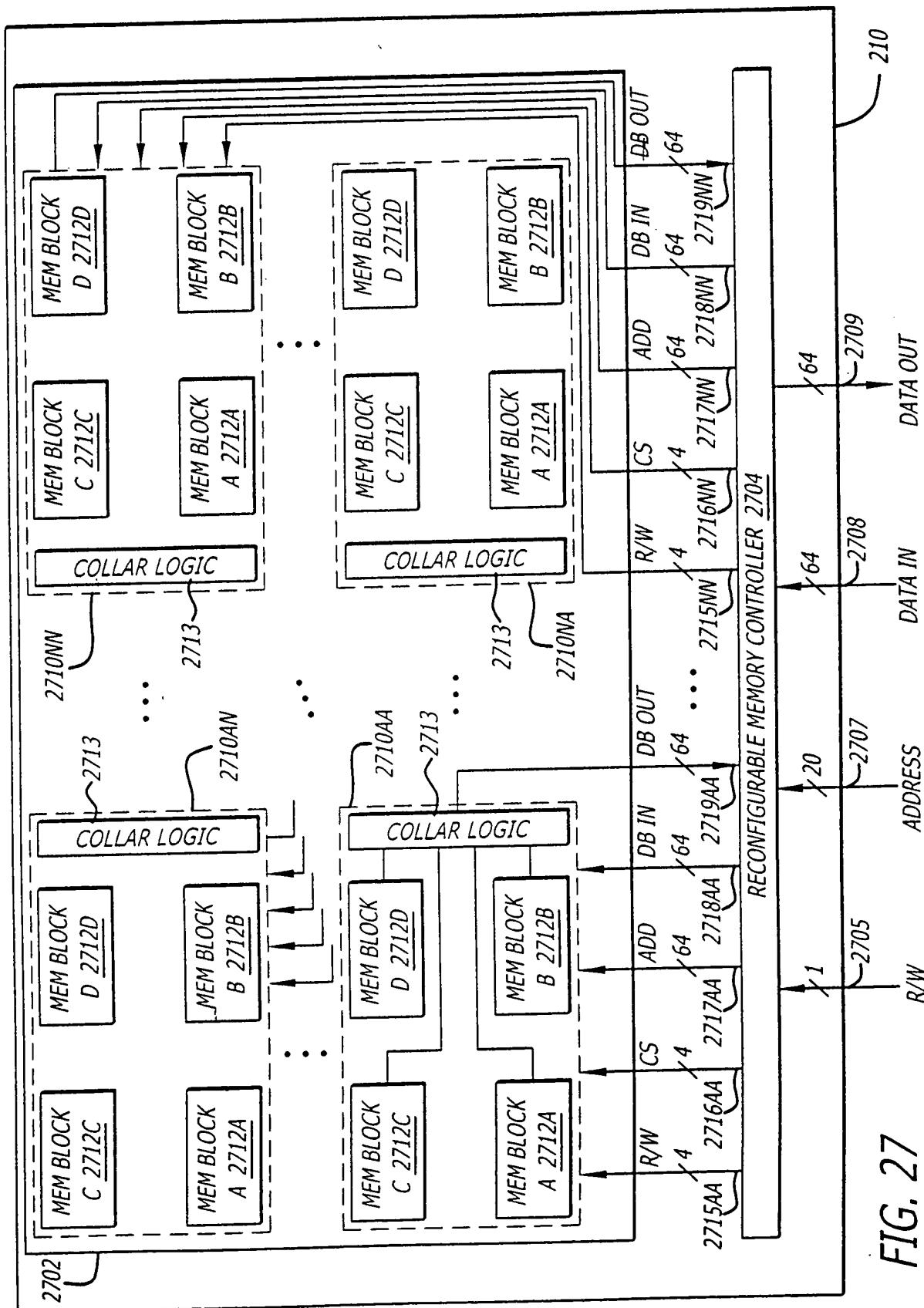


FIG. 27

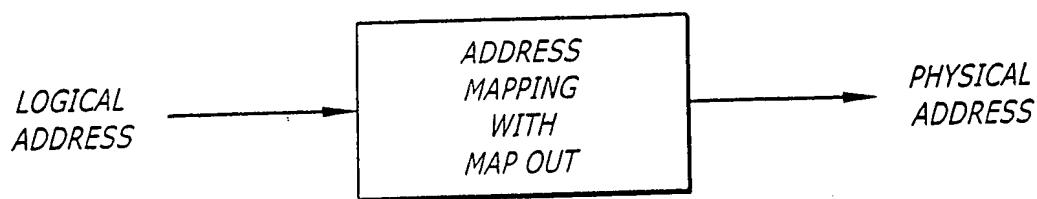


FIG. 28

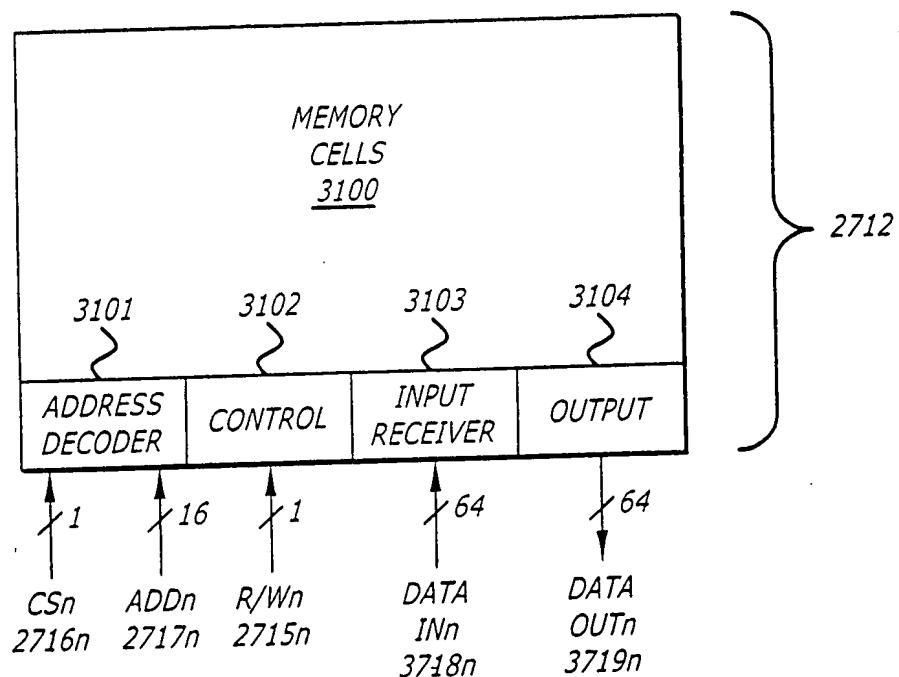


FIG. 31

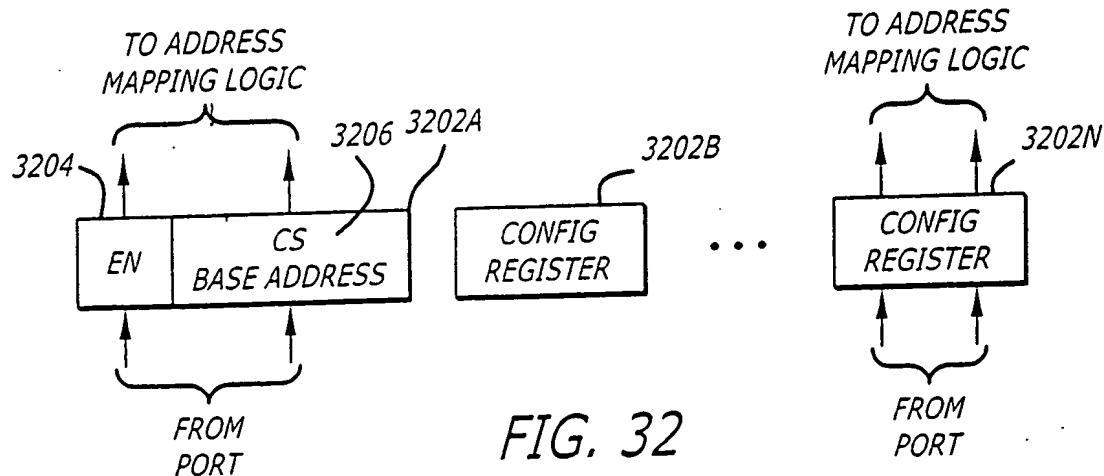
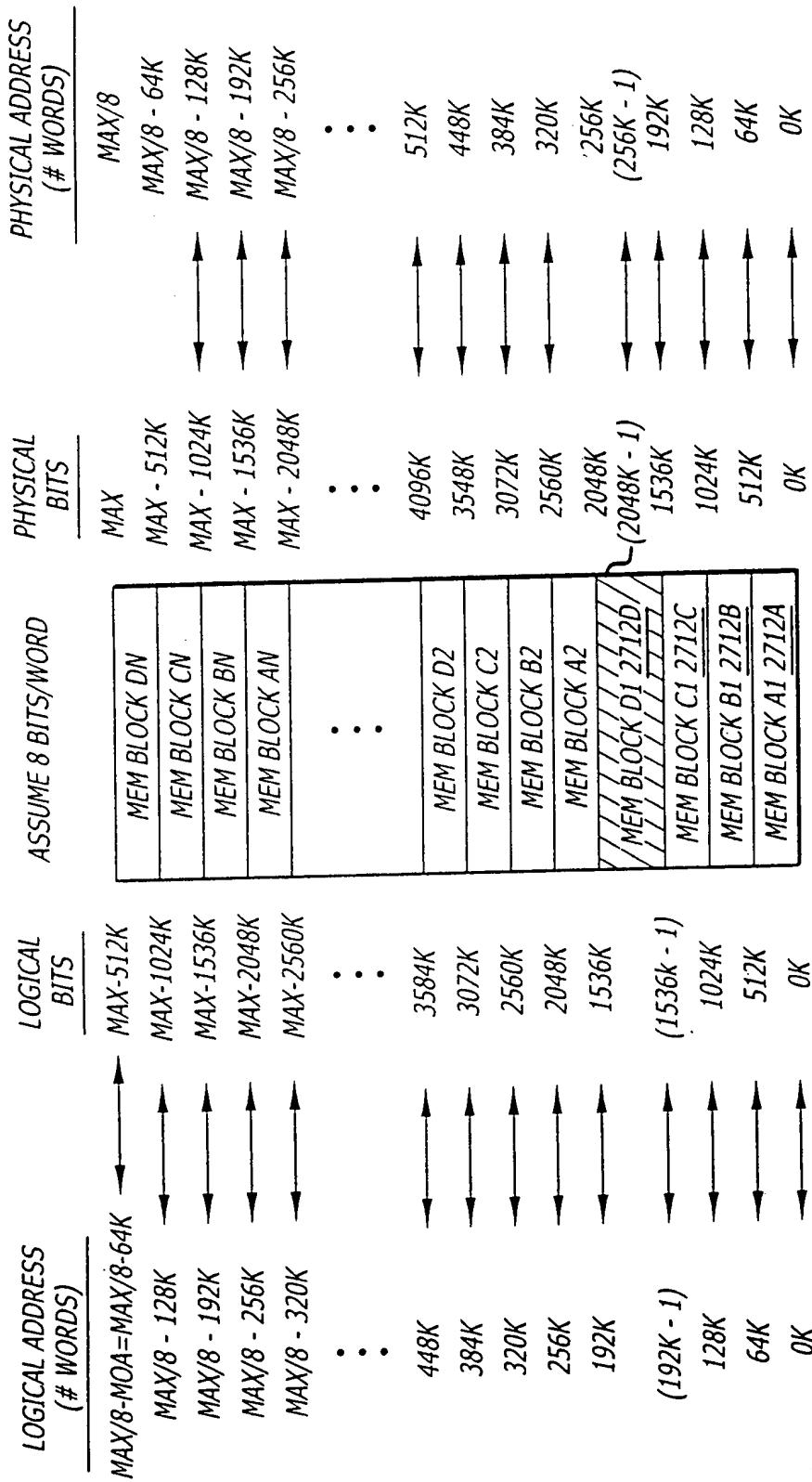


FIG. 32

FIG. 29



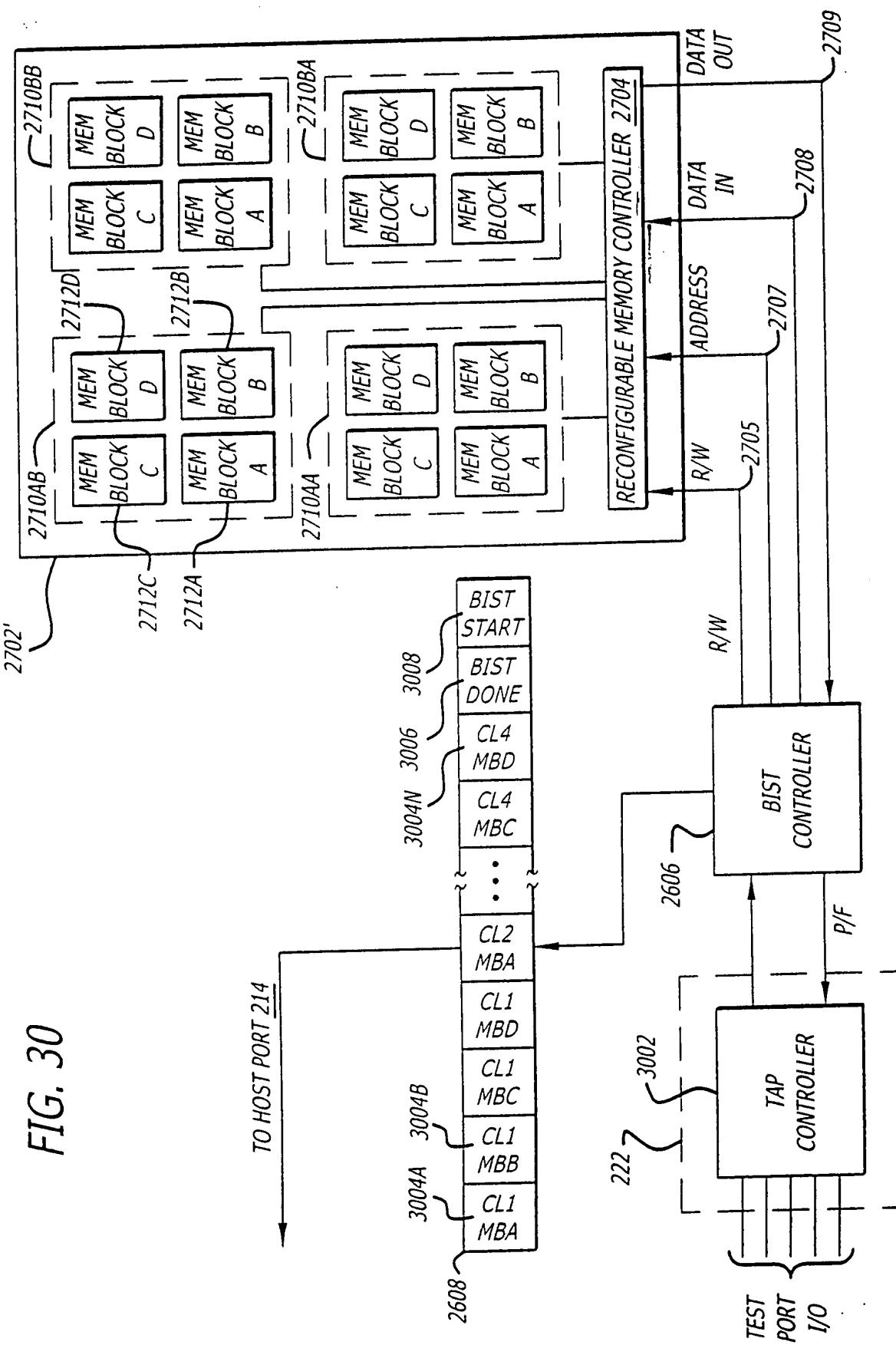
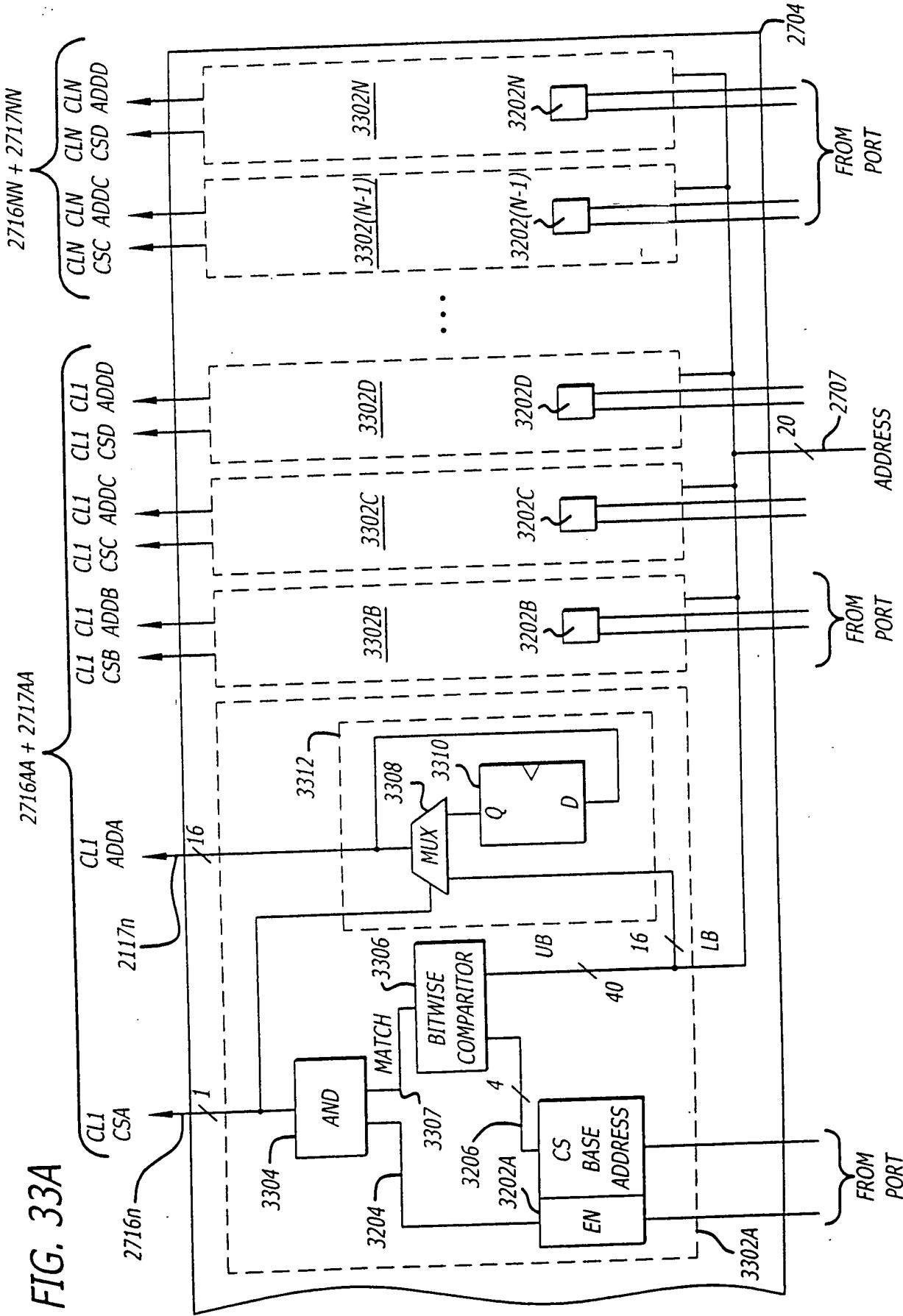
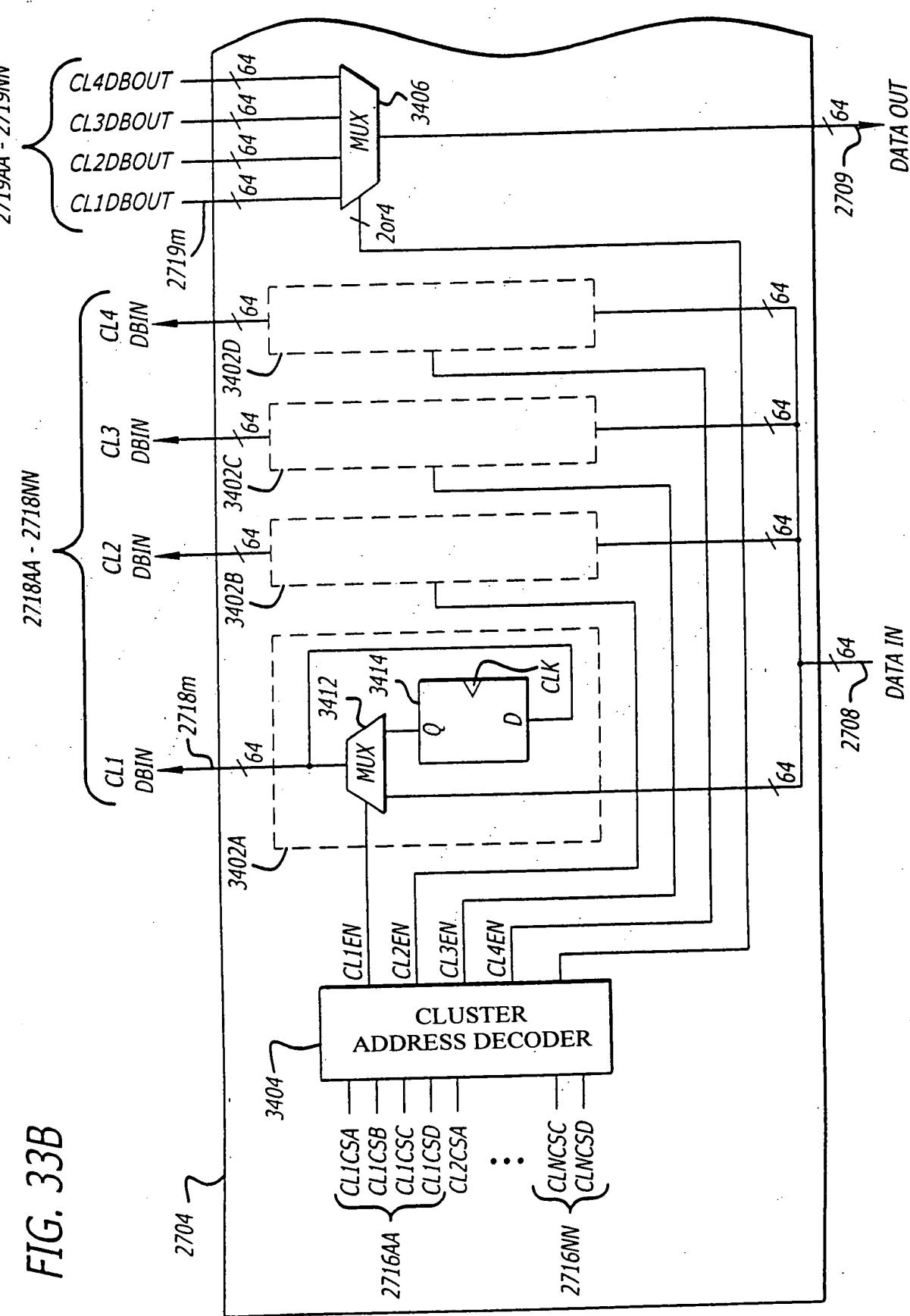
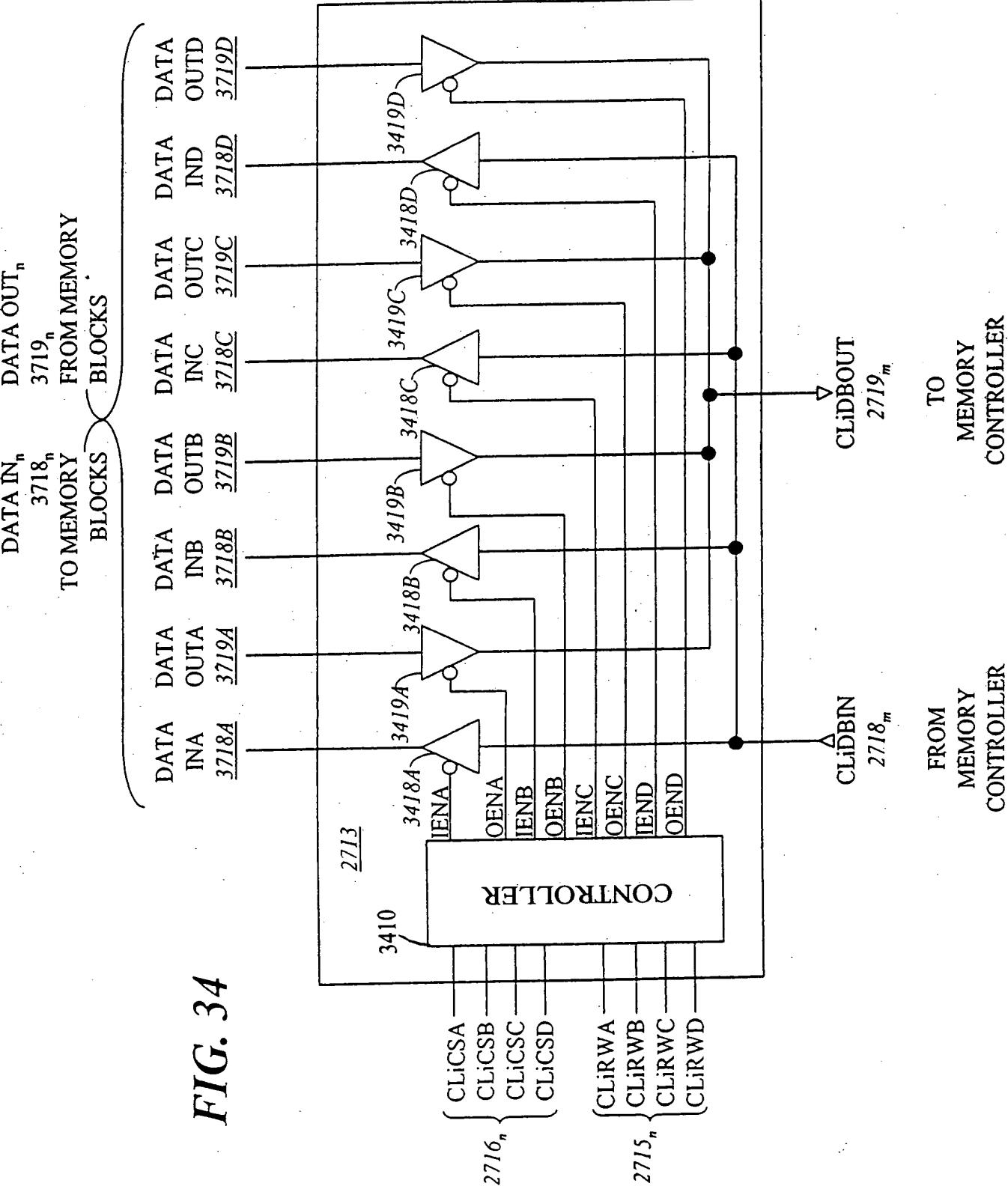


FIG. 33A





DATA IN_n
 3718_n
 TO MEMORY
 BLOCKS



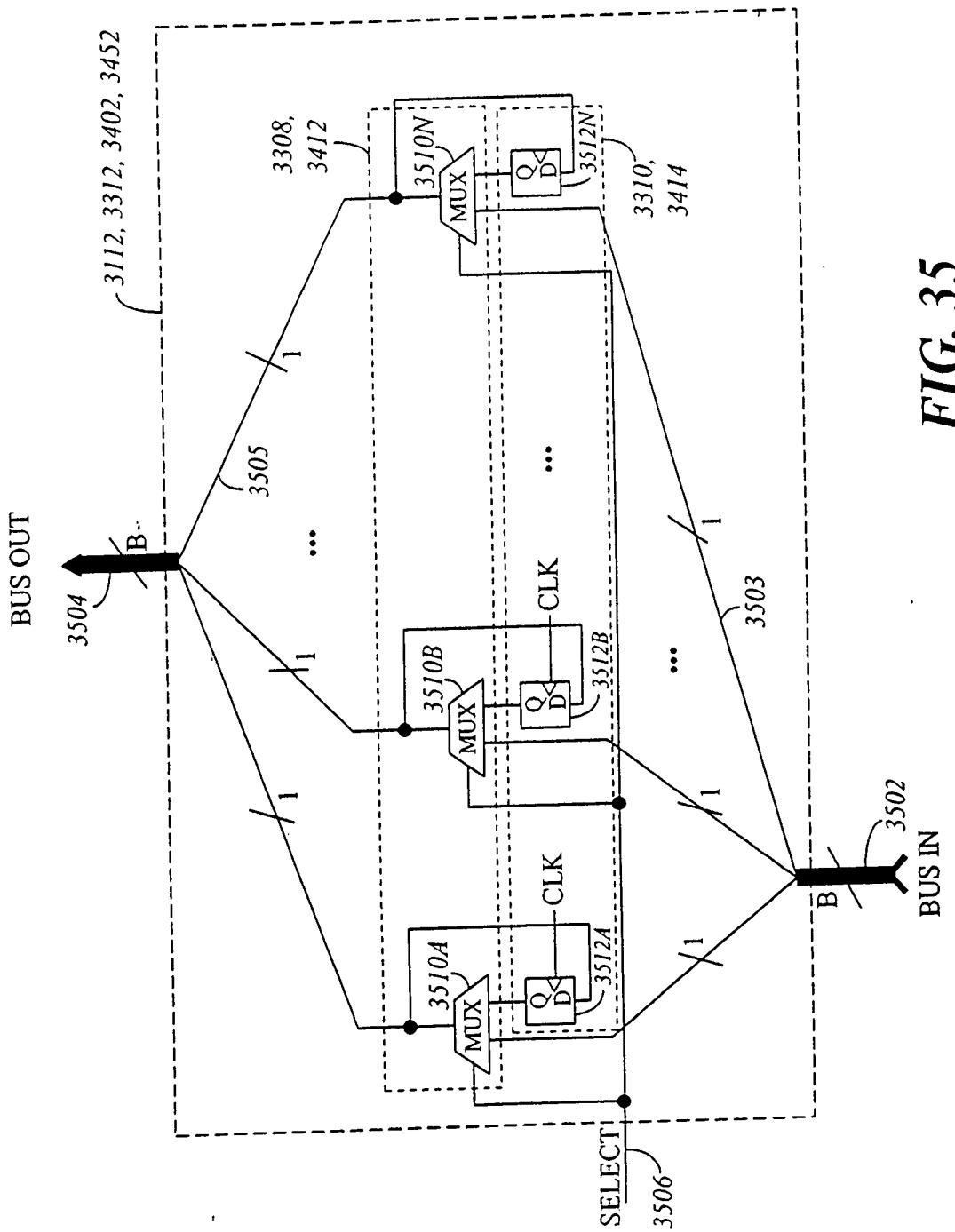


FIG. 35

REPLACEMENT SHEET

REF. REPLACEMENT SHEET
Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT
1st Named Inventor: Ruban Kanapathippillai
Application No.: 10/649,067 Docket No.: 42P14037D2
Sheet: 55/64

Sheet: 55/64

202

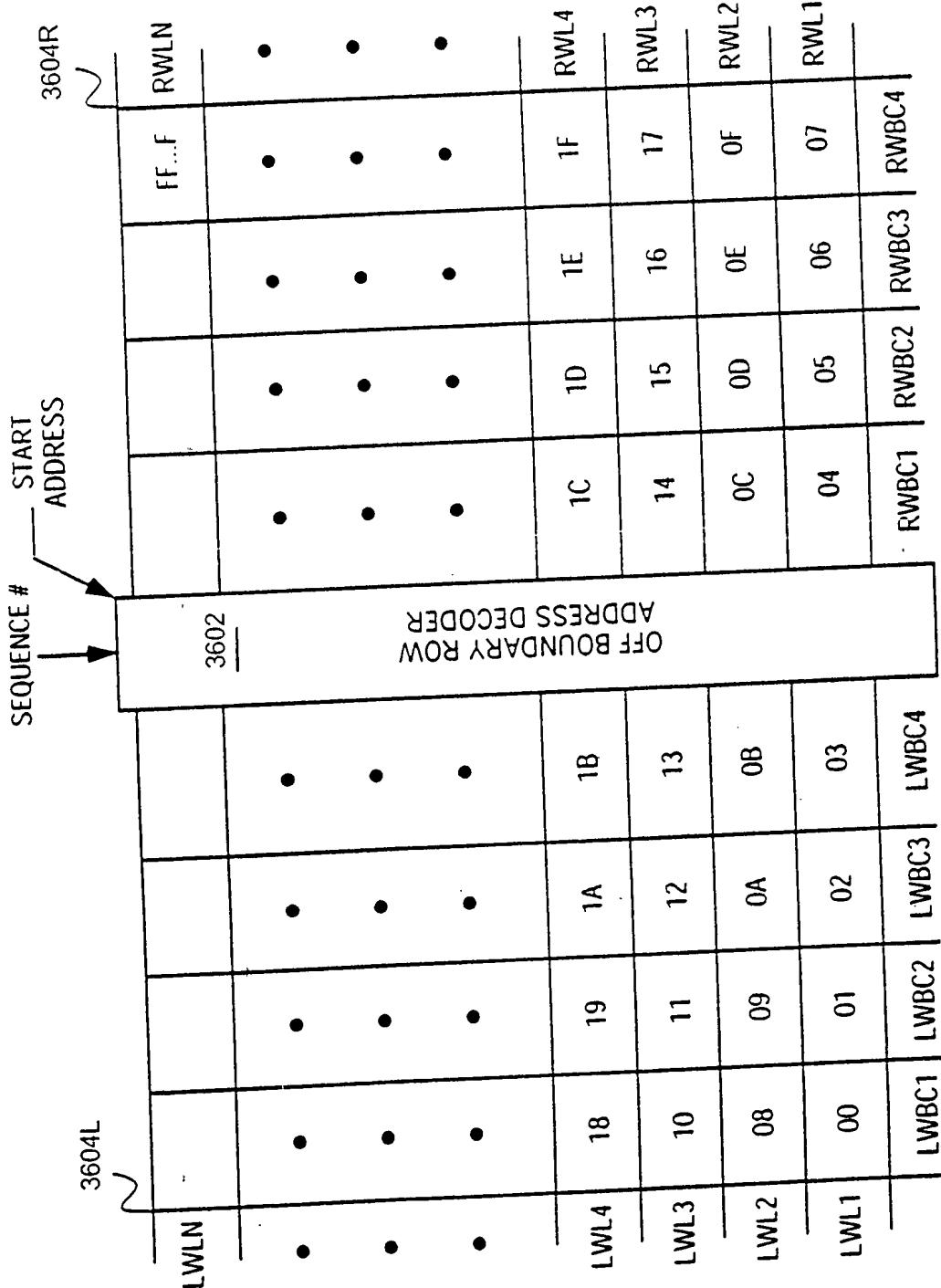


FIG. 36A

REPLACEMENT SHEET

Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT
1st Named Inventor: Ruban Kanapathippillai
Application No.: 10/649,067 Docket No.: 42P14037D2
Sheet: 56/64

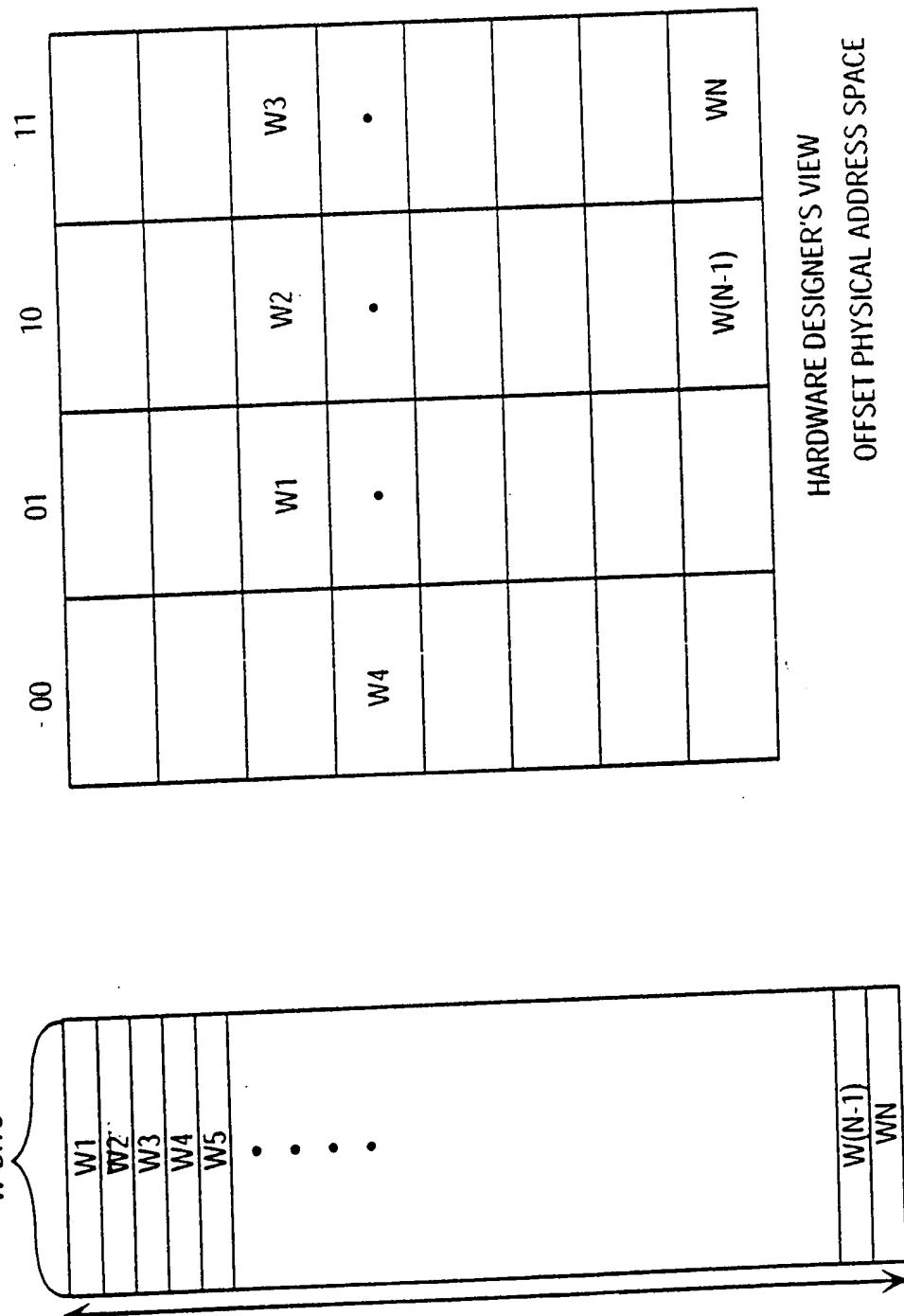


FIG. 36B

PROGRAMMER'S
VIEW

LINEAR
LOGICAL
ADDRESS
SPACE

FIG. 36C

HARDWARE DESIGNER'S VIEW
OFFSET PHYSICAL ADDRESS SPACE

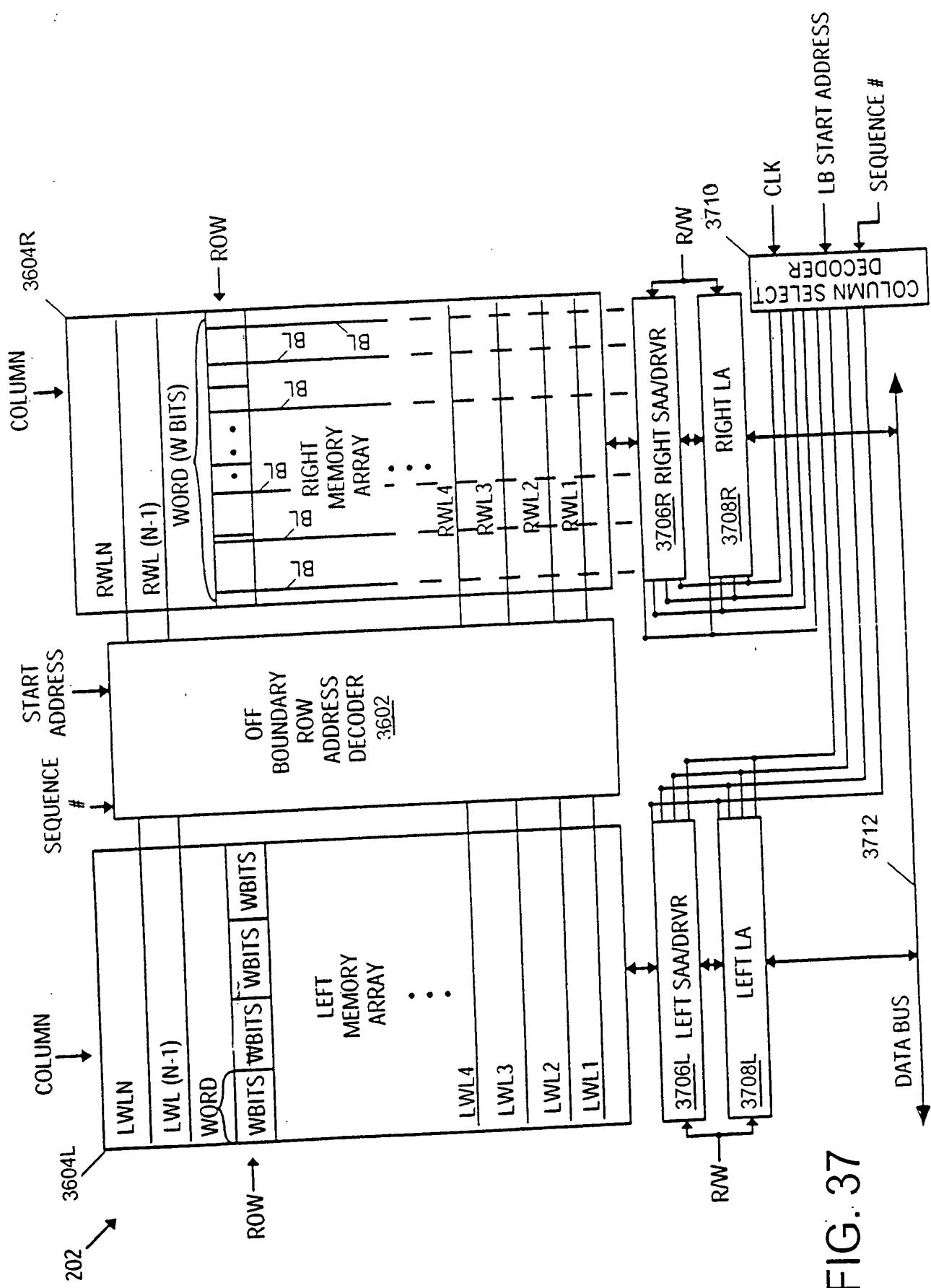


FIG. 37

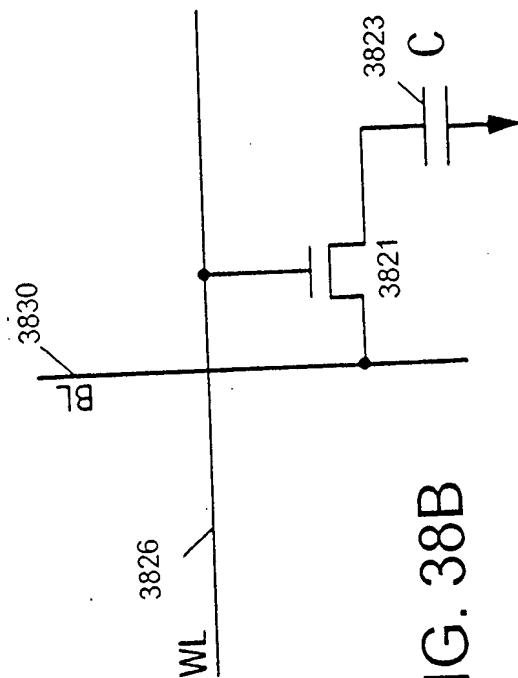


FIG. 38B

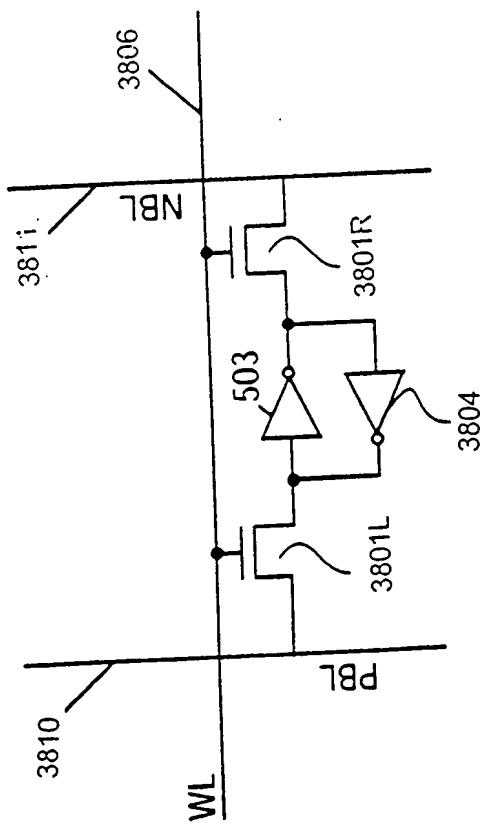


FIG. 38A

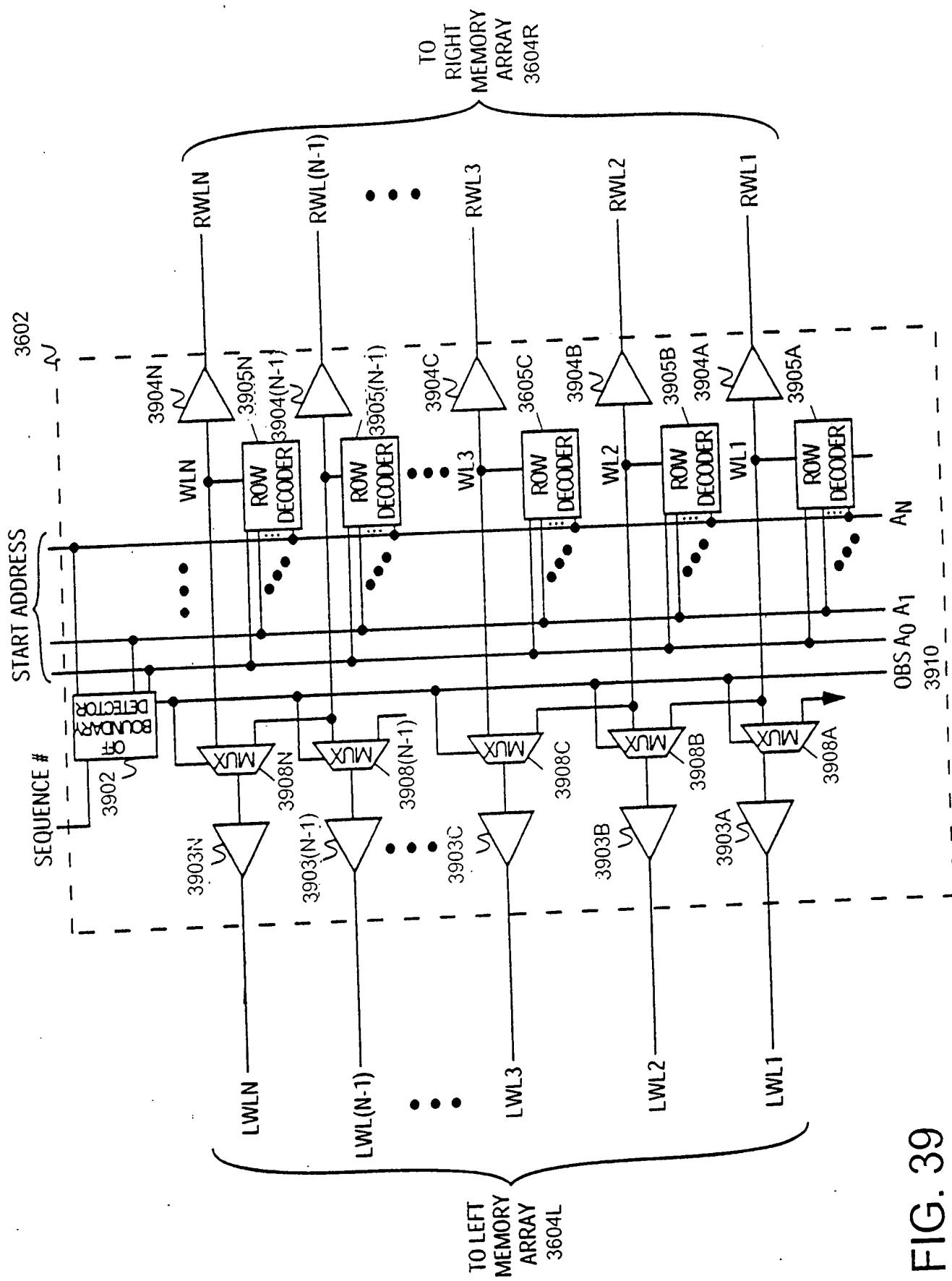


FIG. 39

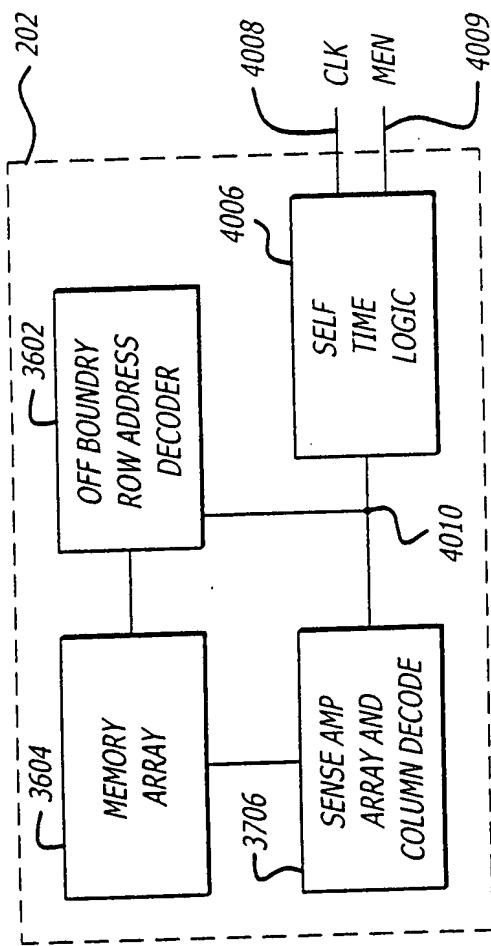


FIG. 40

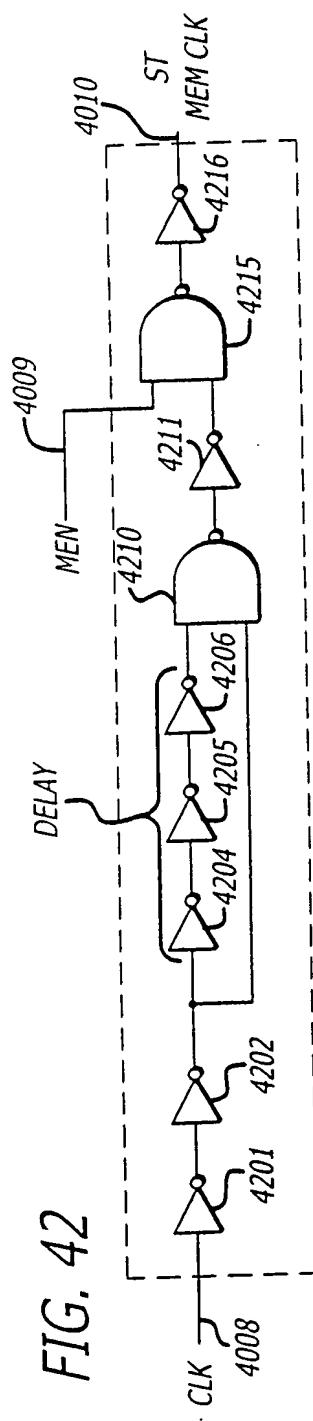


FIG. 42

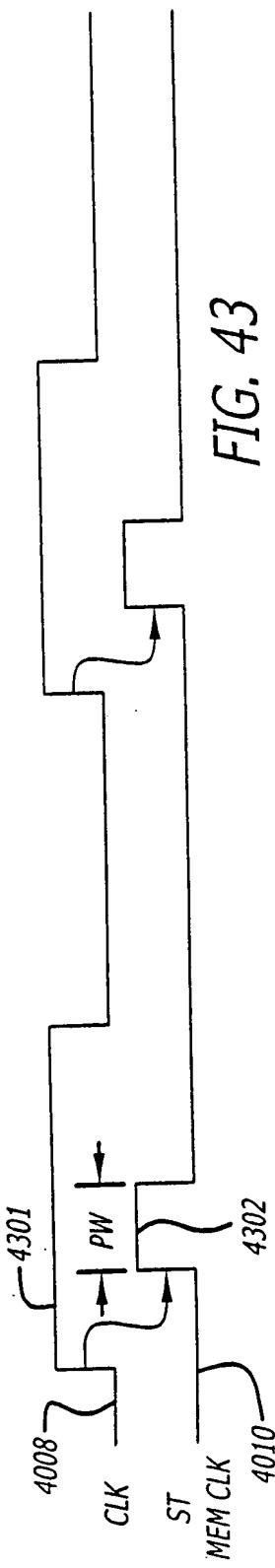
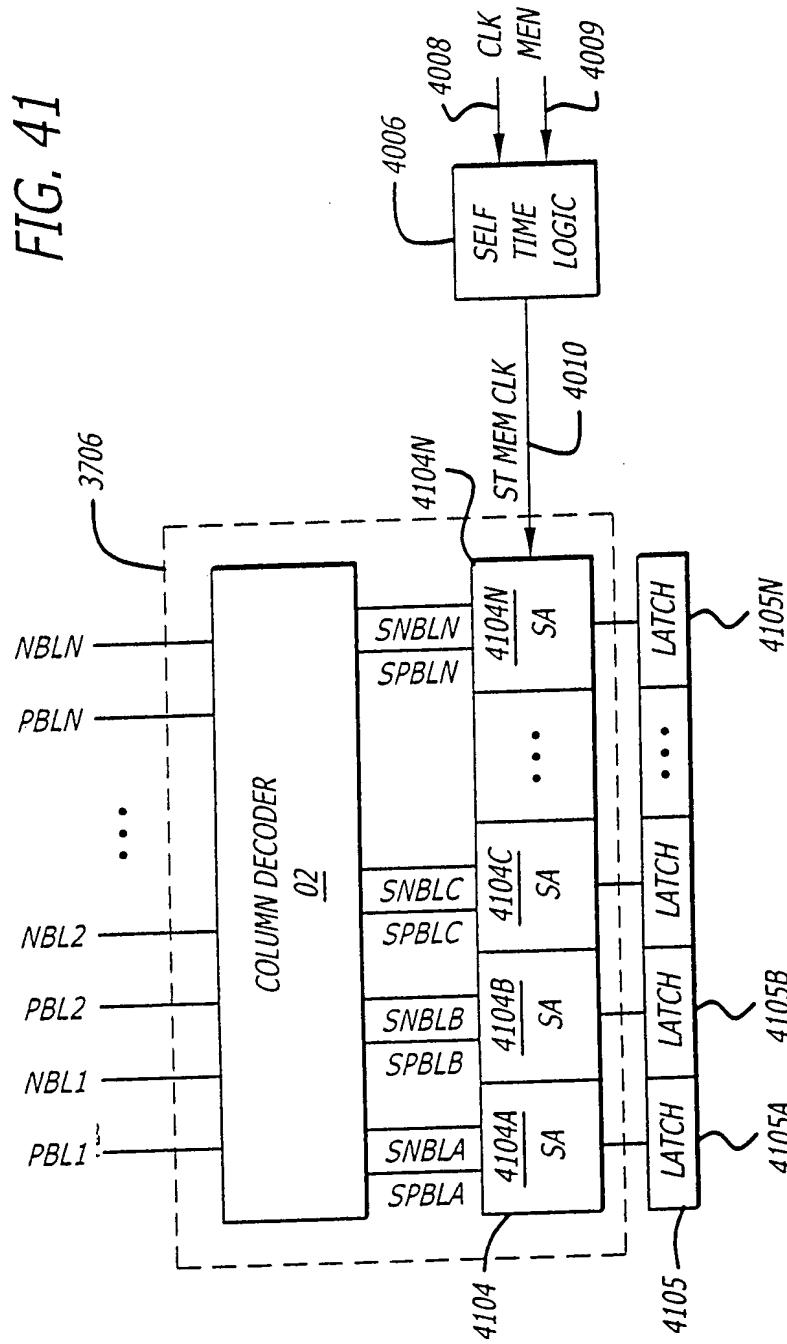


FIG. 43

FIG. 41



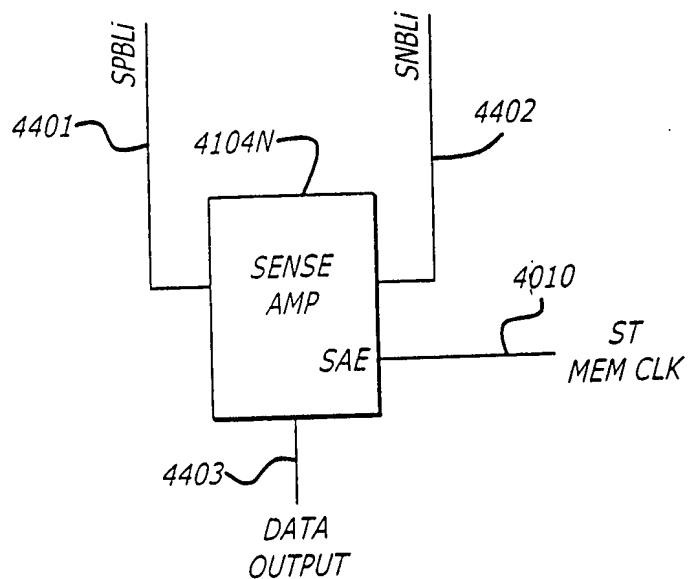


FIG. 44A

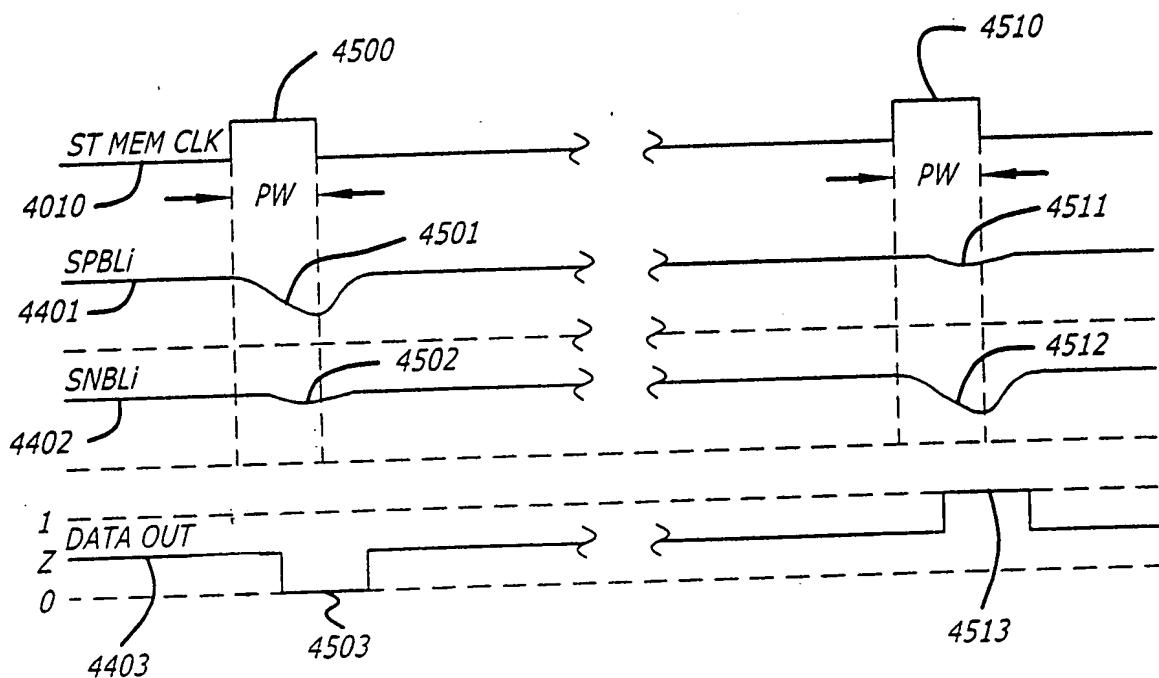


FIG. 45

REPLACEMENT SHEET

REPLACEMENT SHEET
Title: METHOD AND APPARATUS OF BUS STATE KEEPERS FOR
BUSES IN AN INTEGRATED CIRCUIT
1st Named Inventor: Ruban Kanapathippillai
Application No.: 10/649,067 Docket No.: 42P14037D2
Sheet: 63/64

Sheet: 63/64

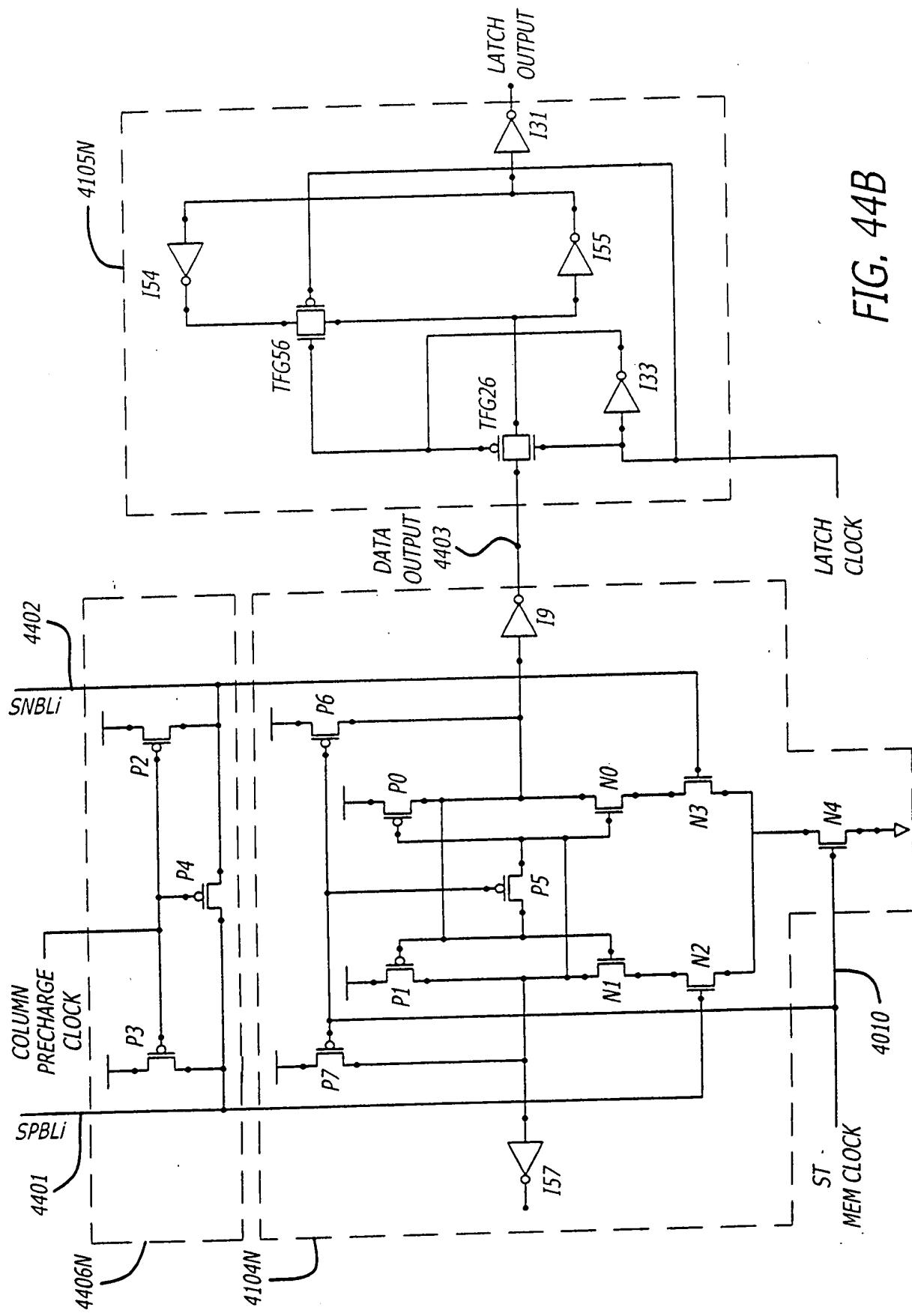


FIG. 44B

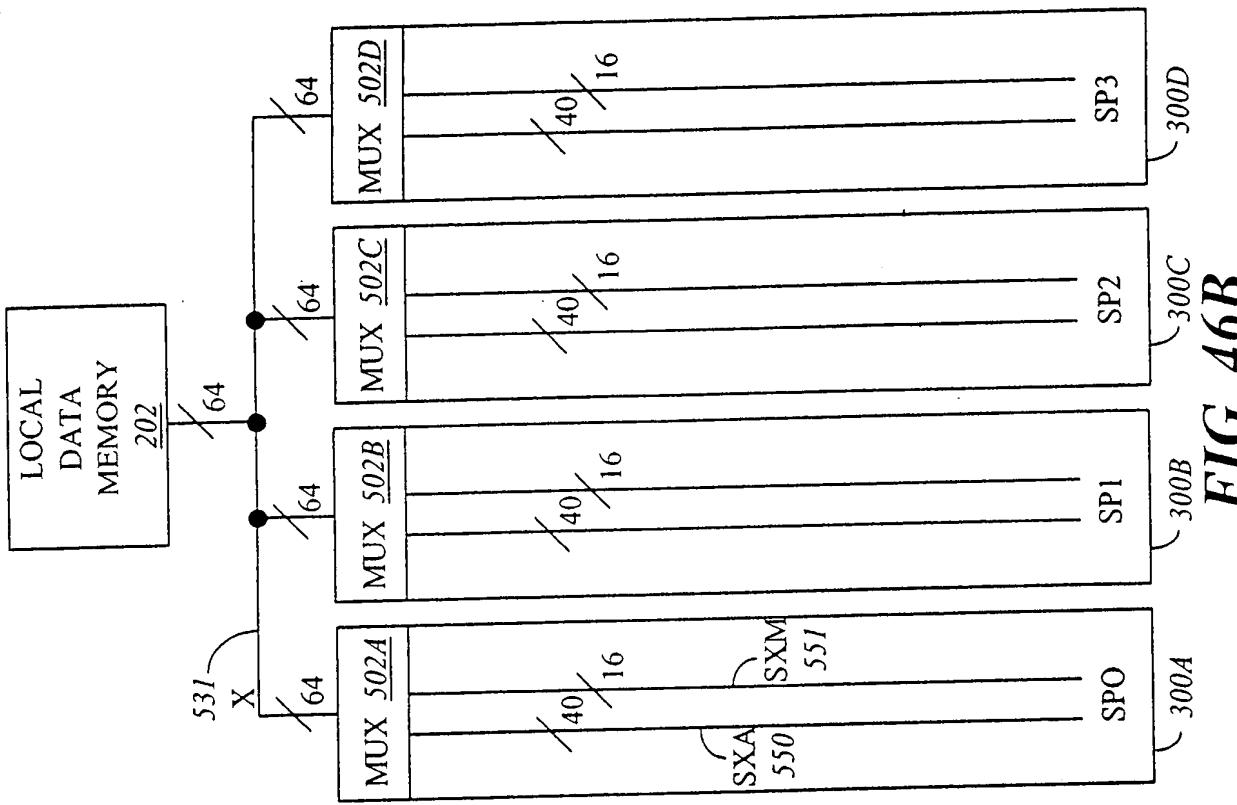


FIG. 46B

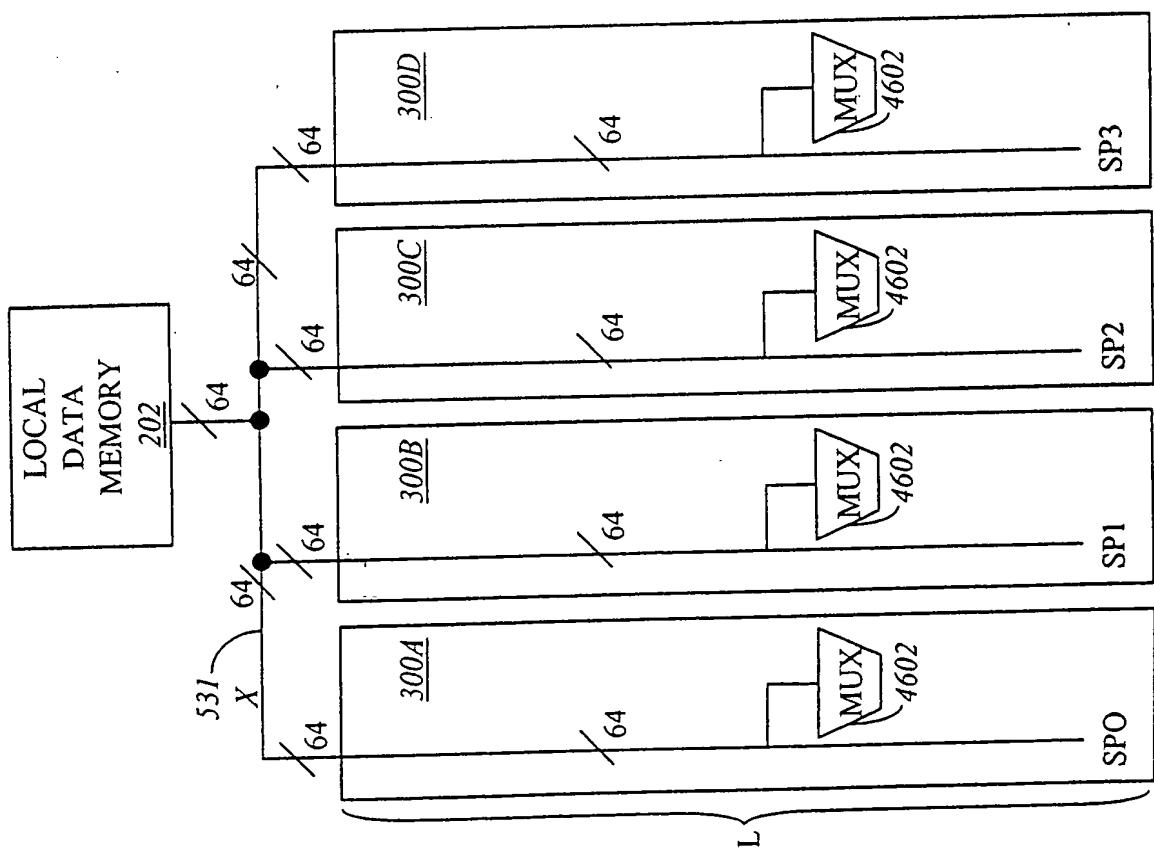


FIG. 46A